

CONFIDENTIAL

Mosaic Schematics Document

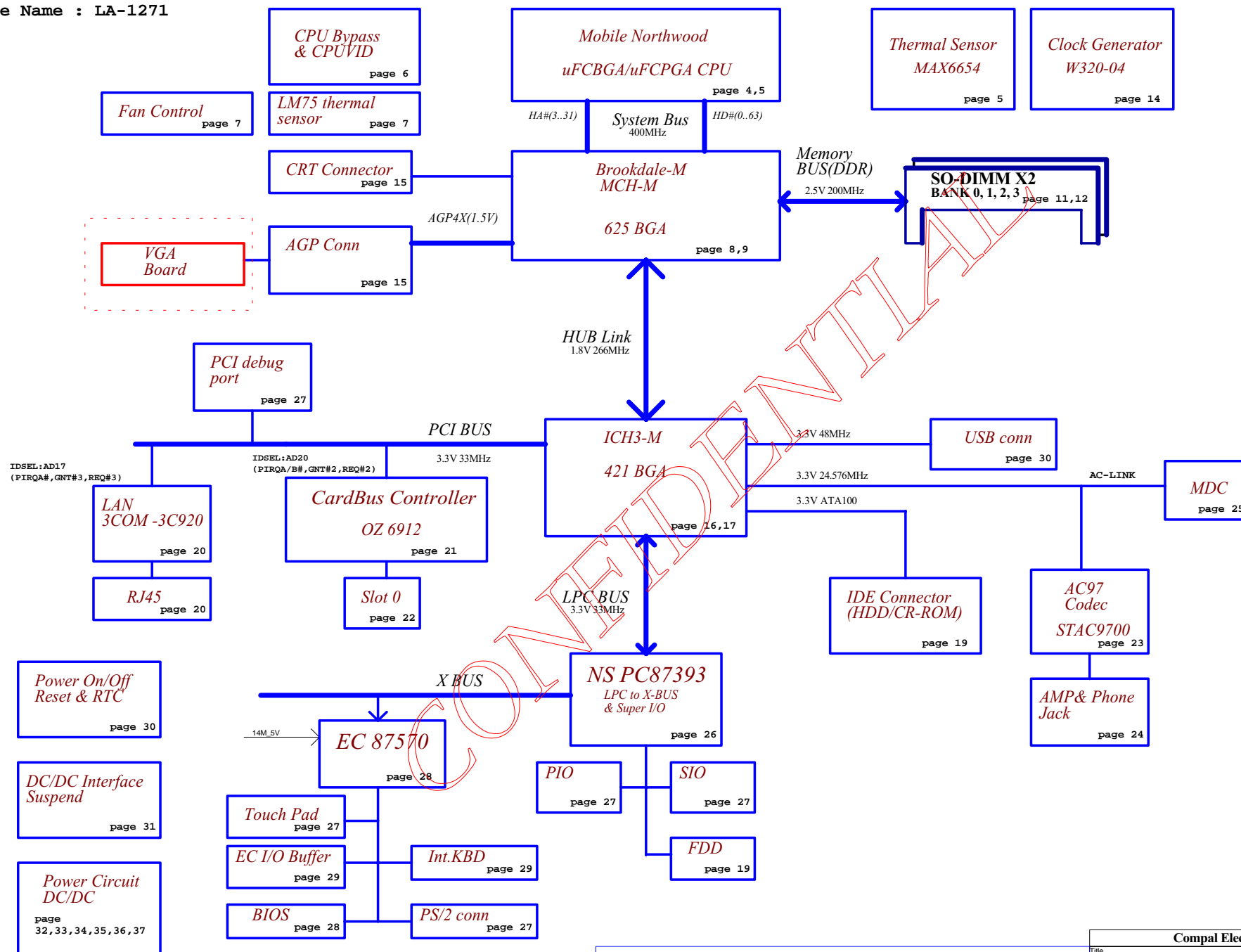
uFCBGA/uFCPGA Northwood

2001-09-19

REV: 0.1

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Compal Electronics, Inc.		
Title		
Cover Sheet		
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Function	Model	Mosaic	Midas
FDD		YES	YES
PS/2		YES	YES
Serial port		NO	NO
Parallel port		YES	YES
RJ45		YES	YES
OZ6912/TPS2211		YES	YES
3Com Lan chipset(3C920)		YES S/W disable	YES

Note1: "@" means all model depop

Note2: Removed serial port,because add 2nd Fan

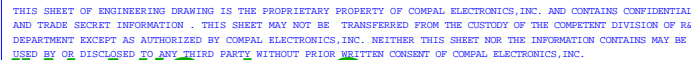
Power Managment table

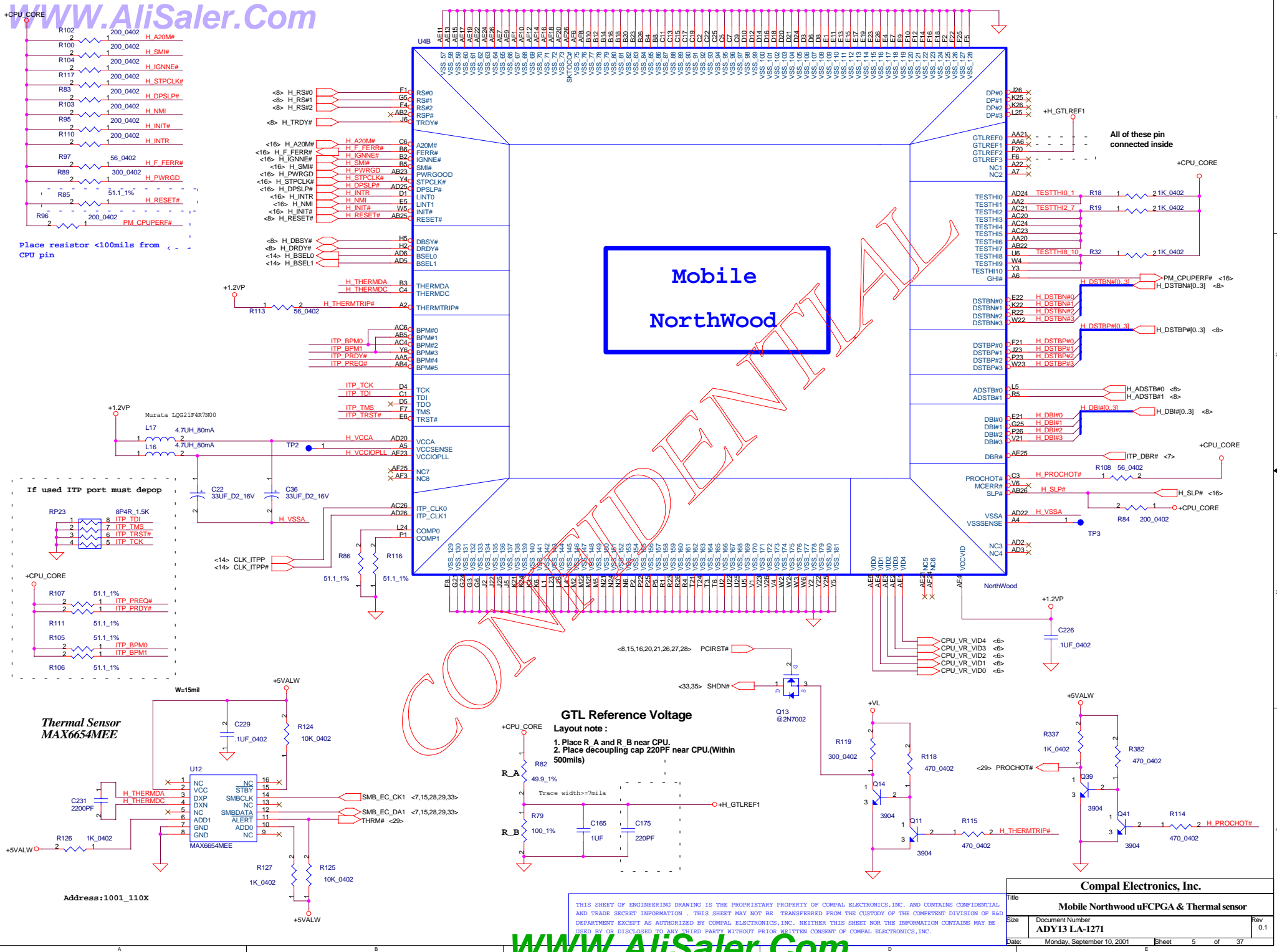
Signal	+3VALW	+3V	+3VS
State	+5VALW	+5V	+5VS
	+1.8VALW	+2.5V	+1.8VS
	+12VALW		+1.5VS
			+1.2VP
			+CPU_CORE
			+1.25V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

SST-Build	CHIPS Rev	CHIPS Rev
	RG82845	FW82801CAM
	A3(QC45)	B1(QC42)

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Compal Electronics, Inc.		
Title	Note & Revision	
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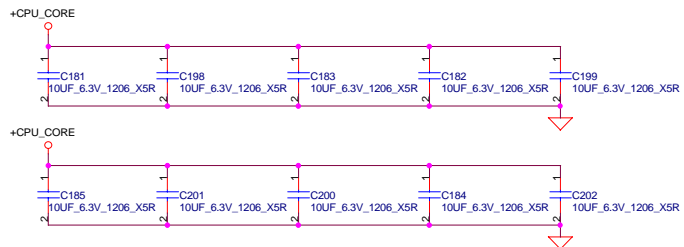




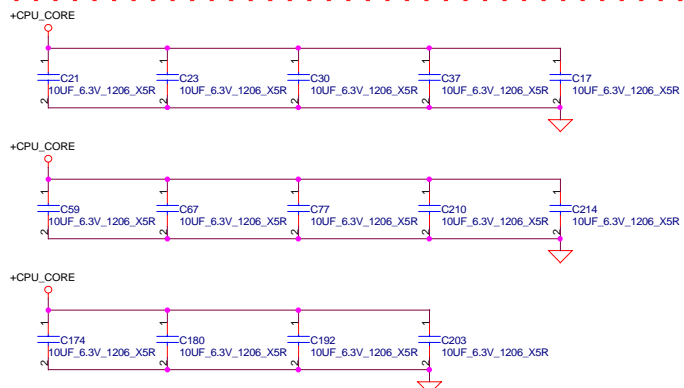
Layout note :

Place close to CPU. Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

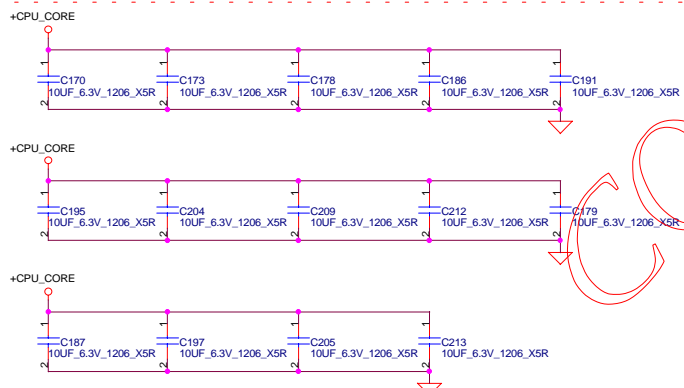
Please place these cap in the socket cavity area



Please place these cap on the socket north side



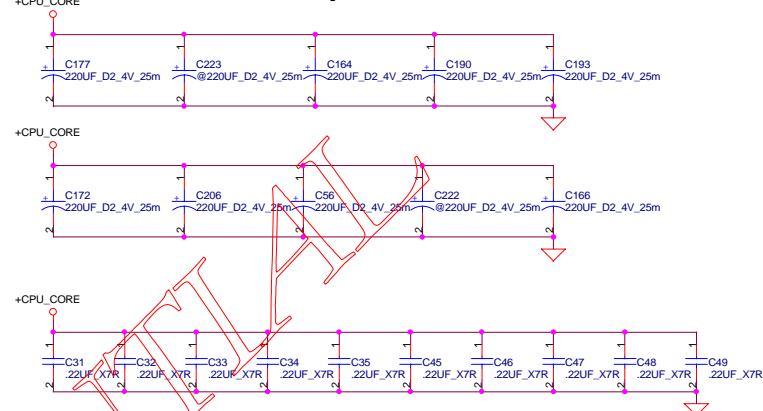
Please place these cap on the socket south side



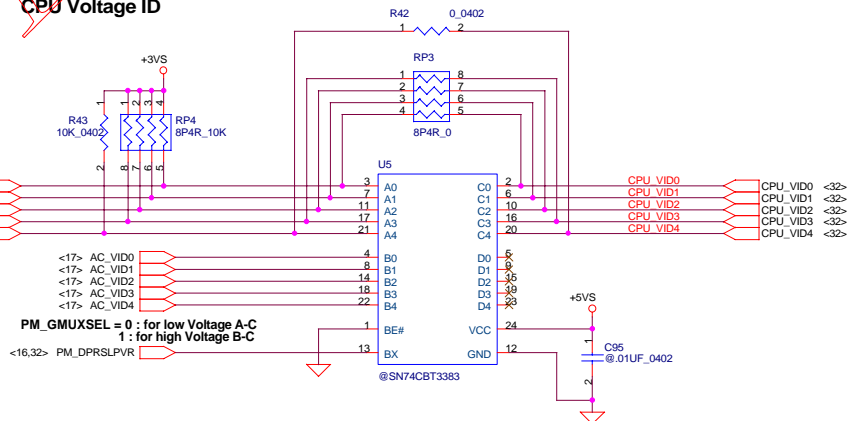
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

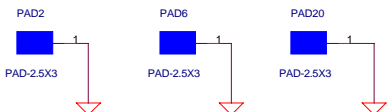
Used ESR 25m ohm cap total ESR=2.5m ohm



CPU Voltage ID



EMI Clip PAD for CPU

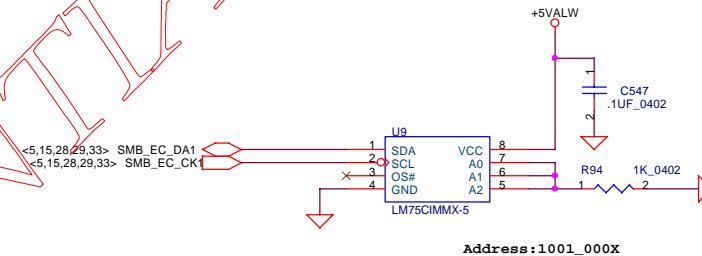
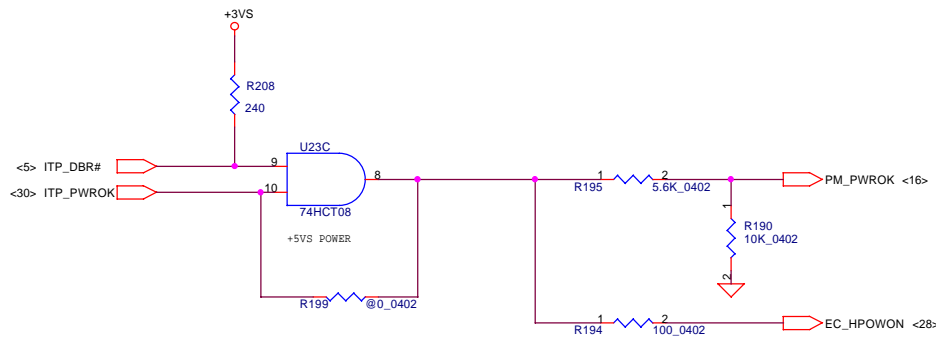


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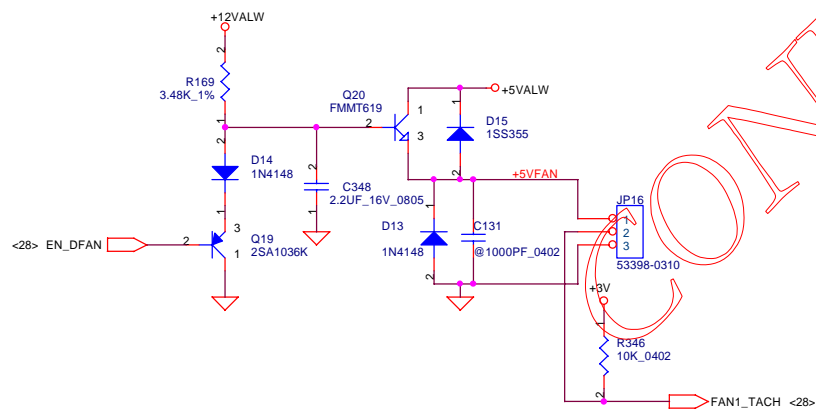
Compal Electronics, Inc.

CPU Bypass & CPU VID

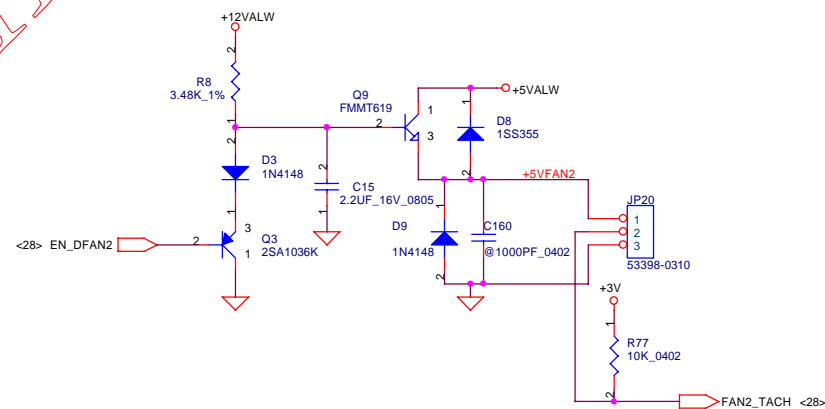
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Fan1 Control circuit

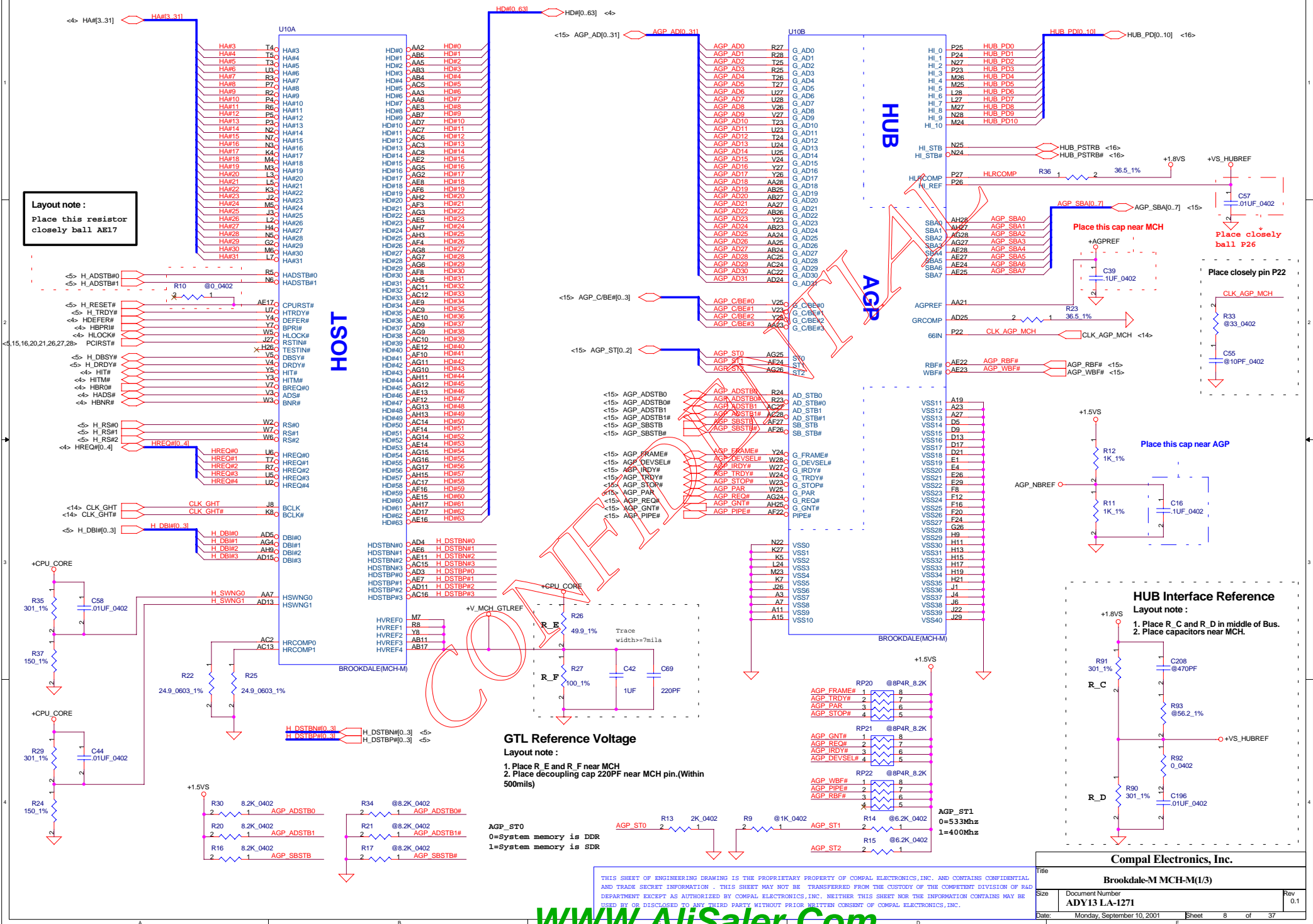


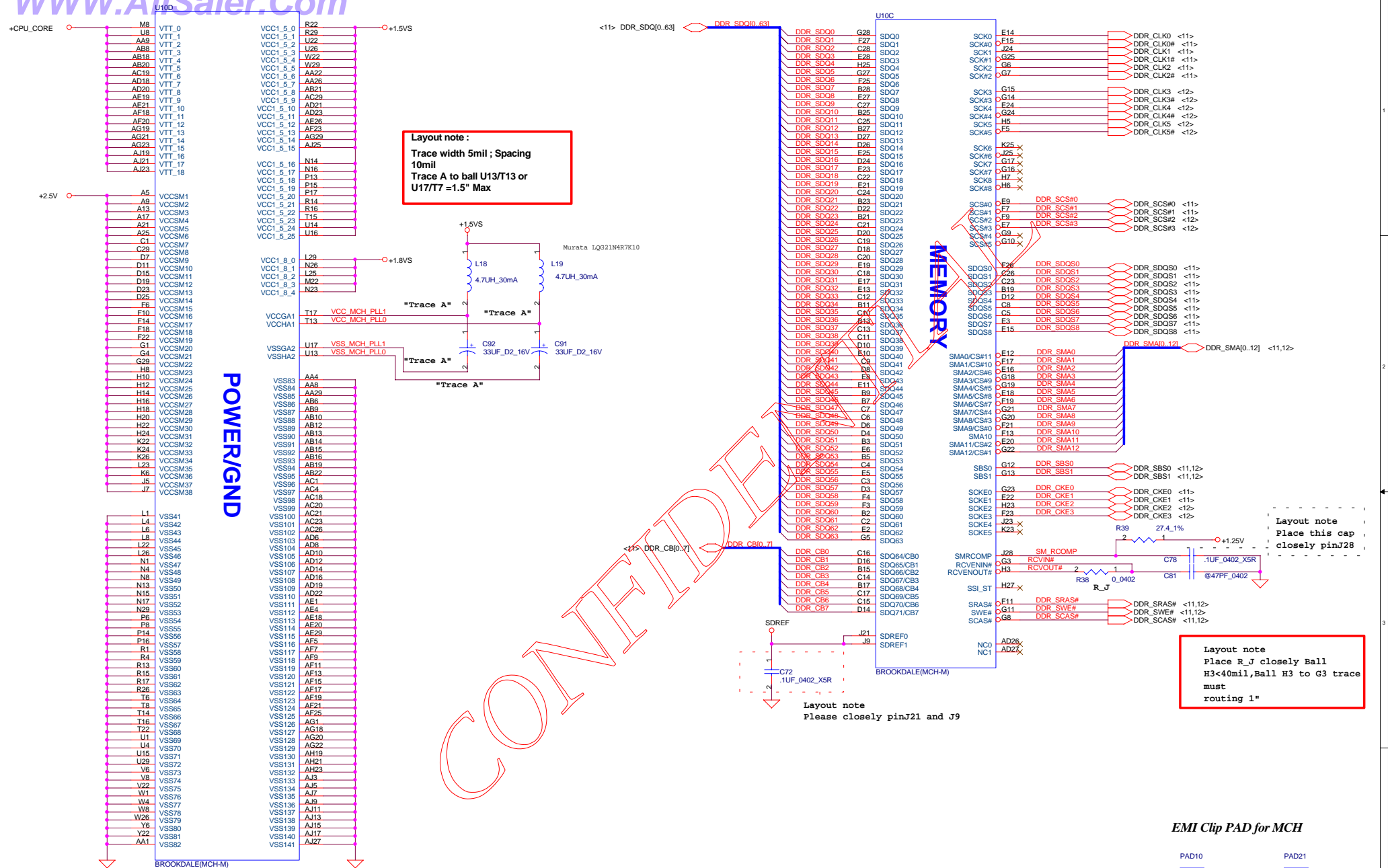
Fan2 Control circuit



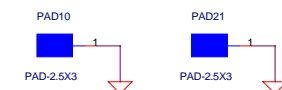
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COMPAL Electronics, Inc			
Title	LM75 Thermal sensor & Fan control		
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EMI Clip PAD for MCH

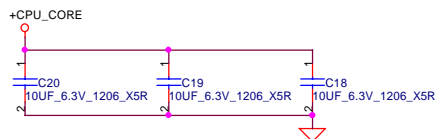
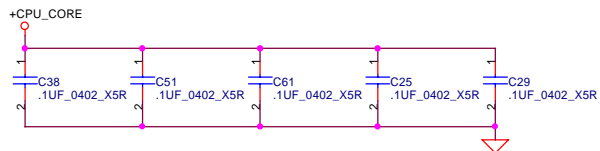
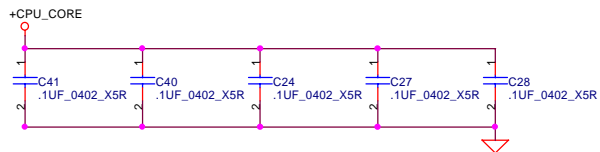


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Compal Electronics, Inc.			
Title			
Brookdale-M MCH-M(2/3)			
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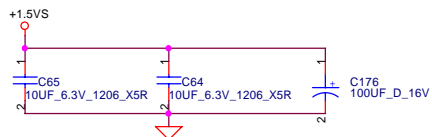
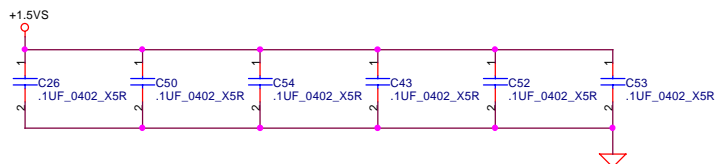
Layout note : Processor system bus

Distribute as close as possible
to MCH Processor Quadrant.(between VTTFB and VSS pin)



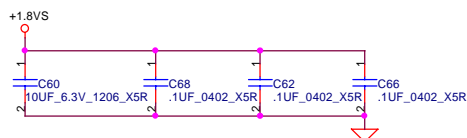
Layout note : AGP / CORE

Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)



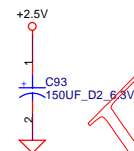
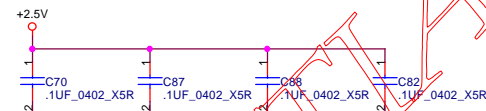
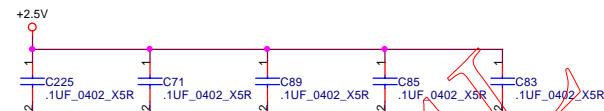
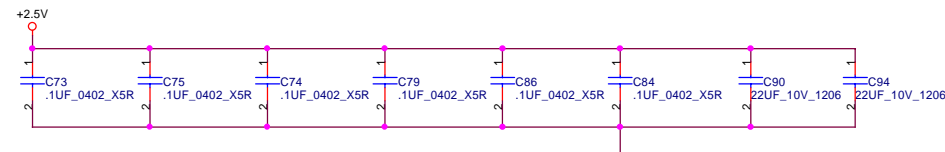
Layout note : Hub-Link

Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)



Layout note : DDR Memory interface

Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)



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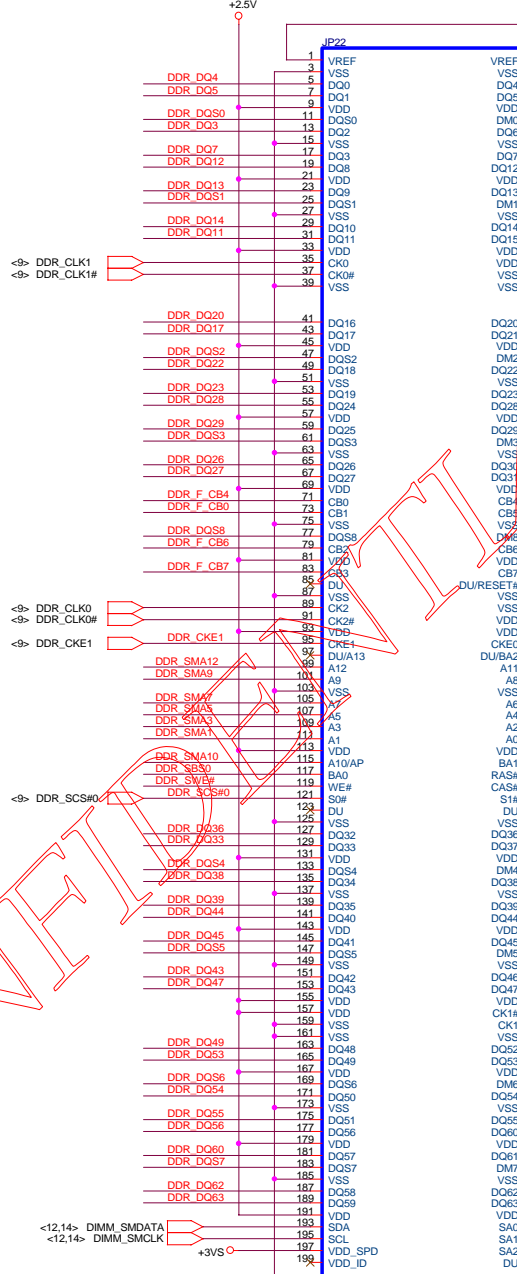
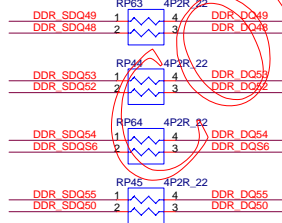
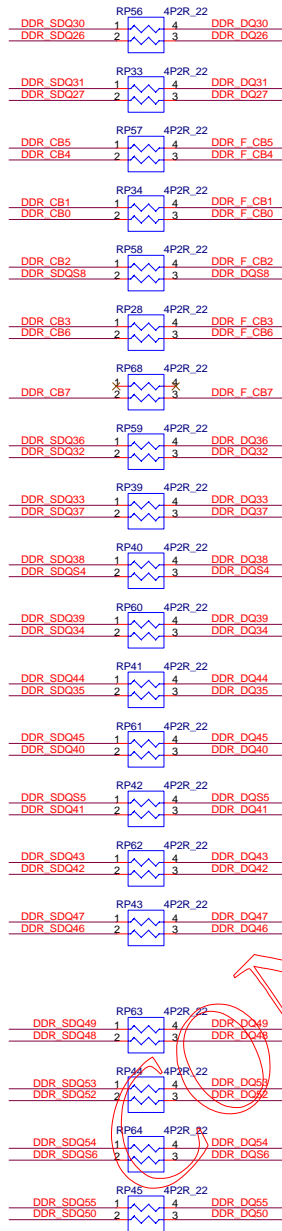
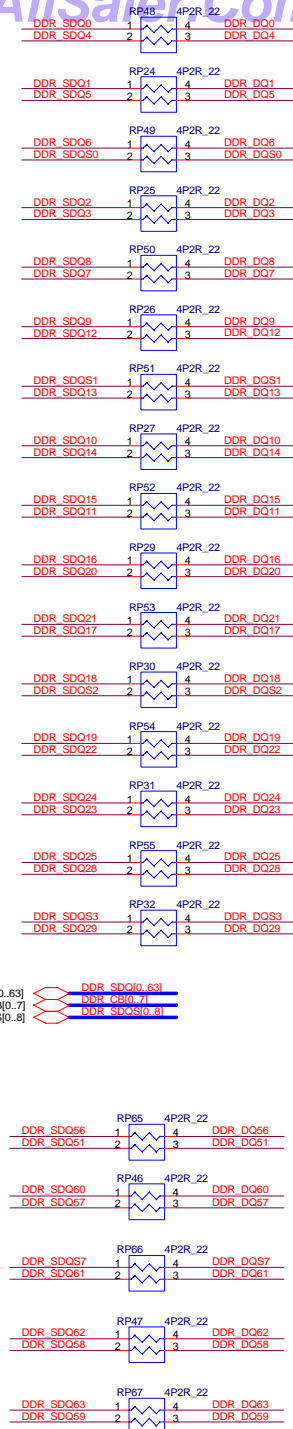
Title	MCH-M Decoupling		
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Layout note

Place these resistor closely DIMM0, all trace length<750mil

DDR_SQ0[0..63] DDR_SQ0[0..63]
DDR_CB0[0..7] DDR_CB0[0..7]
DDR_SQ0[0..8] DDR_SQ0[0..8]

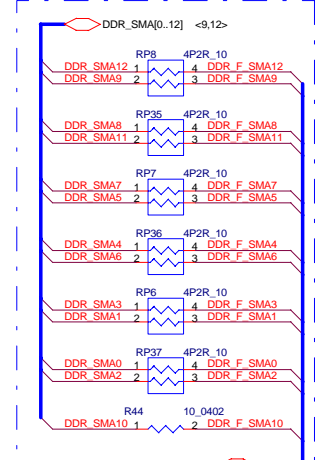


DIMM0

Bottom side

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DDR_DQ0[0..63] DDR_DQ0[0..63]
DDR_F_CB0[0..7] DDR_F_CB0[0..7]
DDR_DQS0[0..8] DDR_DQS0[0..8]

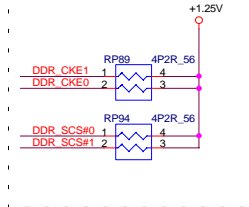


Layout note

Place these resistor closely DIMM0, all trace length<750mil

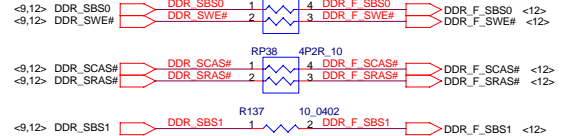
Layout note

Place these resistor closely DIMM0, all trace length Max=1.3"



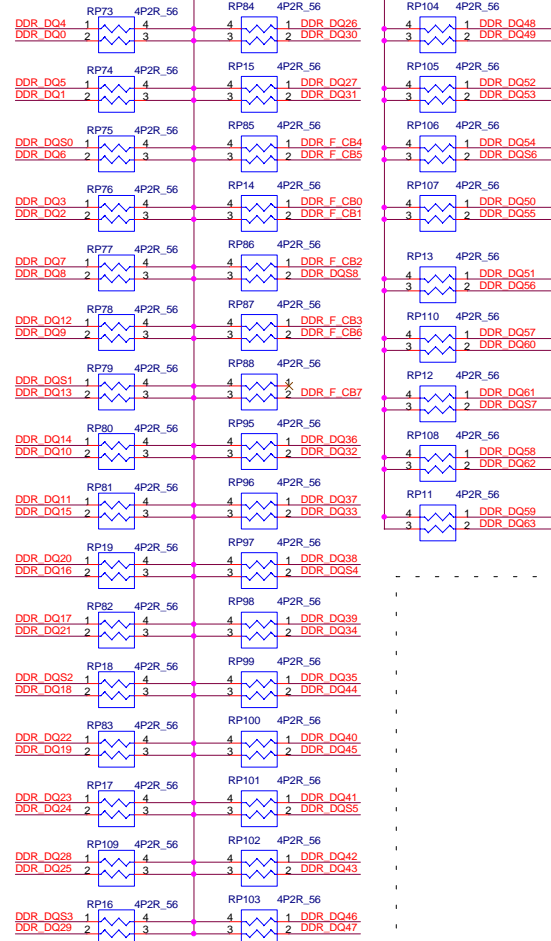
Layout note

Place these resistor closely DIMM0, all trace length<750mil

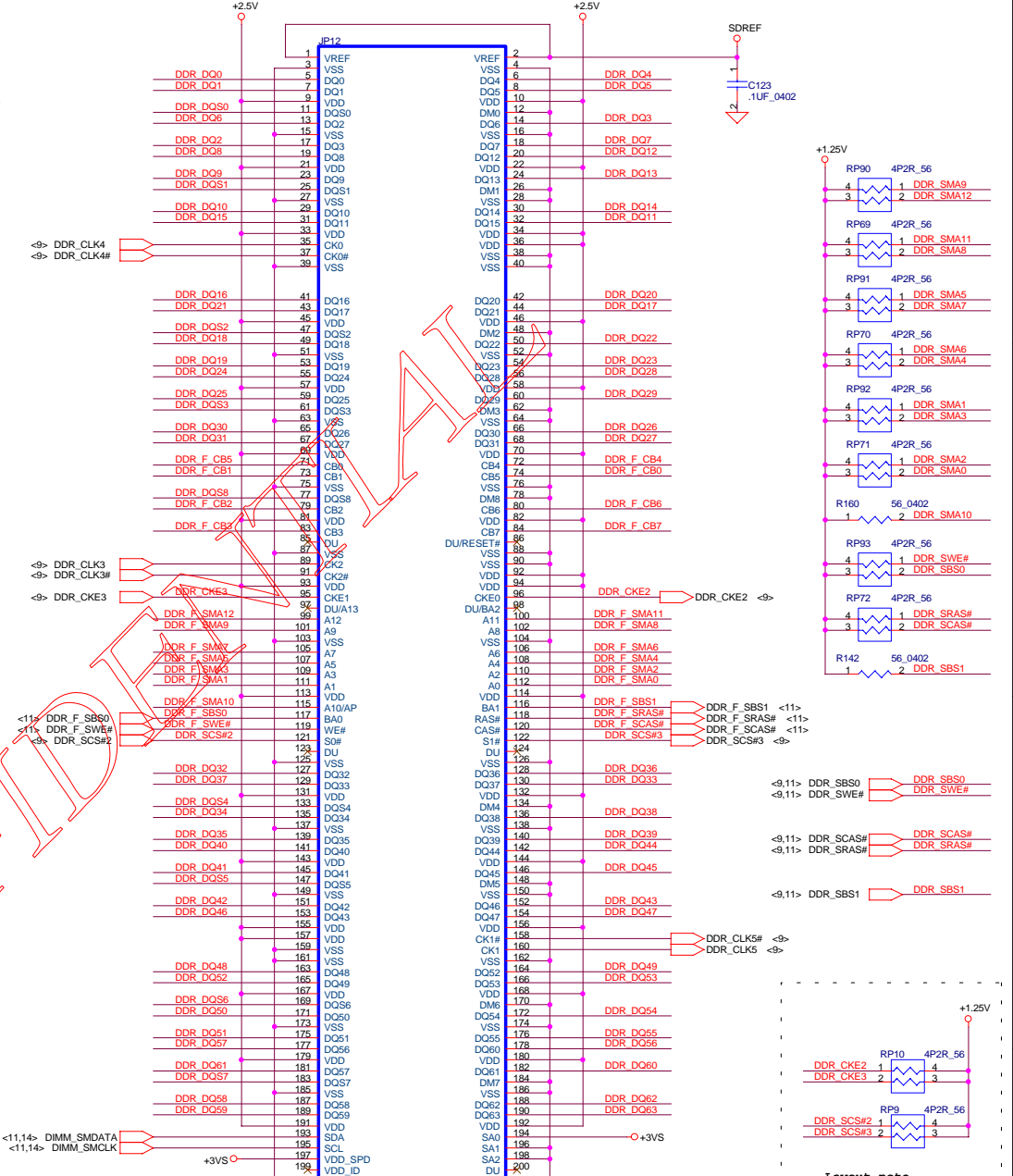
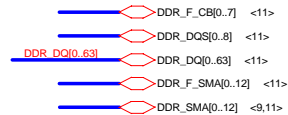


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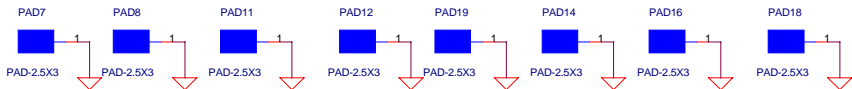
Title		DDR-SODIMM SLOT1	
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Layout note
Place these resistor
closely DIMM1,
all trace
length<=800mil

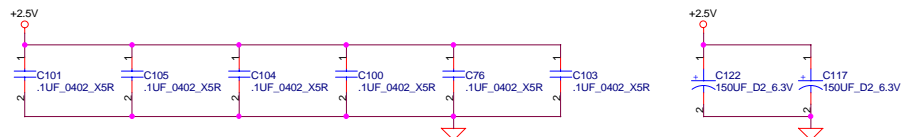
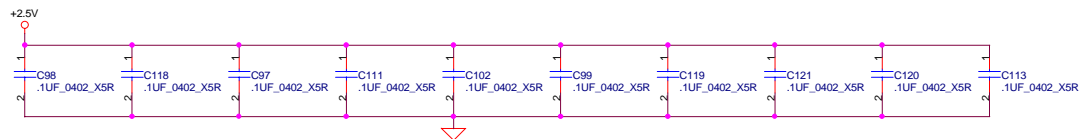


DIMM1
Top side

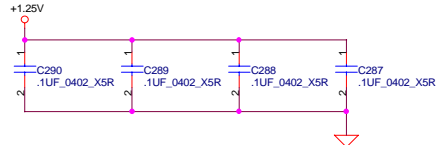
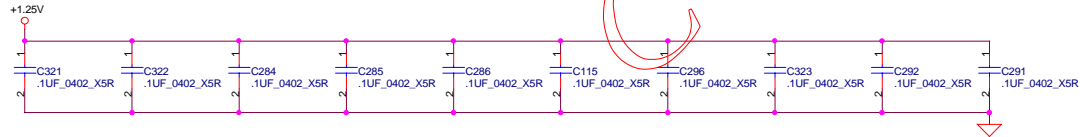
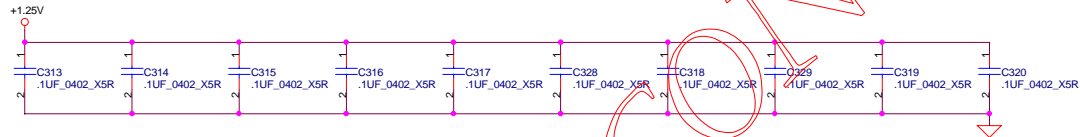
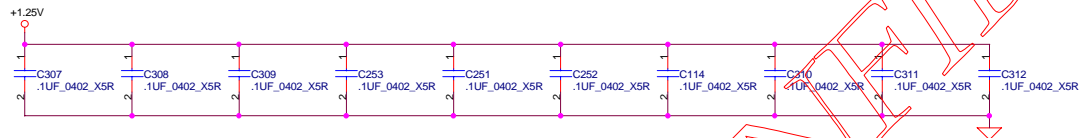
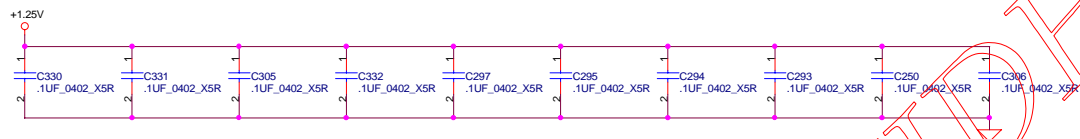
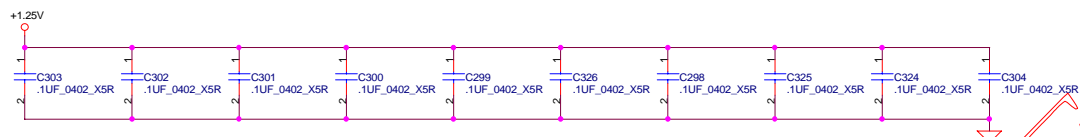


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Layout note :
Distribute as close as possible
to DDR-SODIMM.



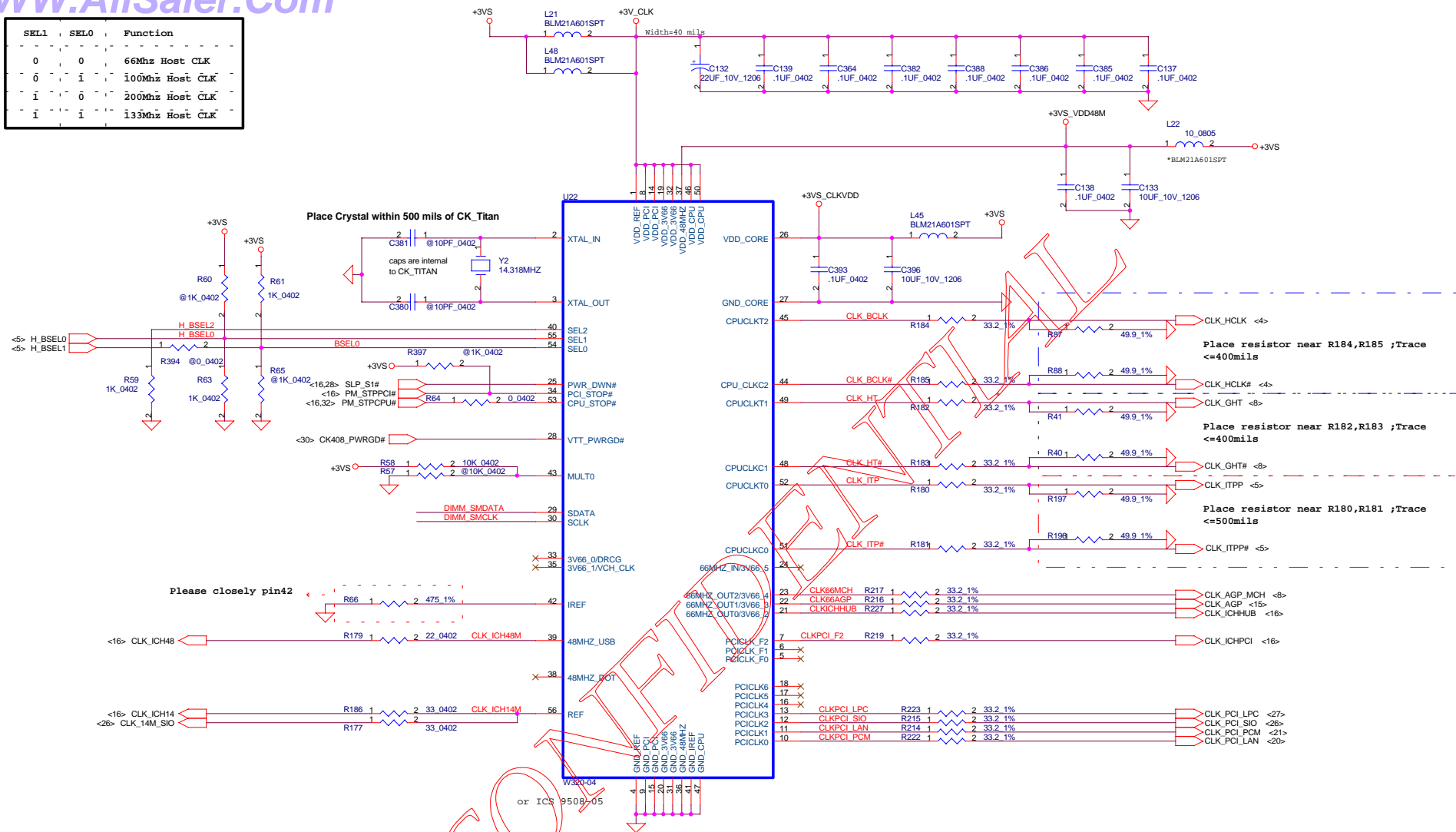
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



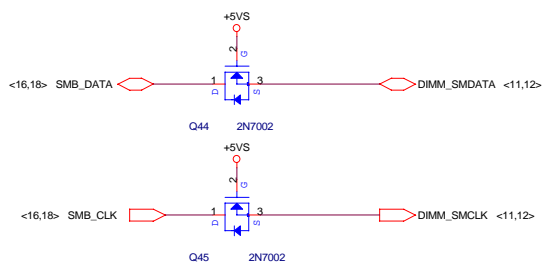
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Title	DDR SODIMM Decoupling		
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SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



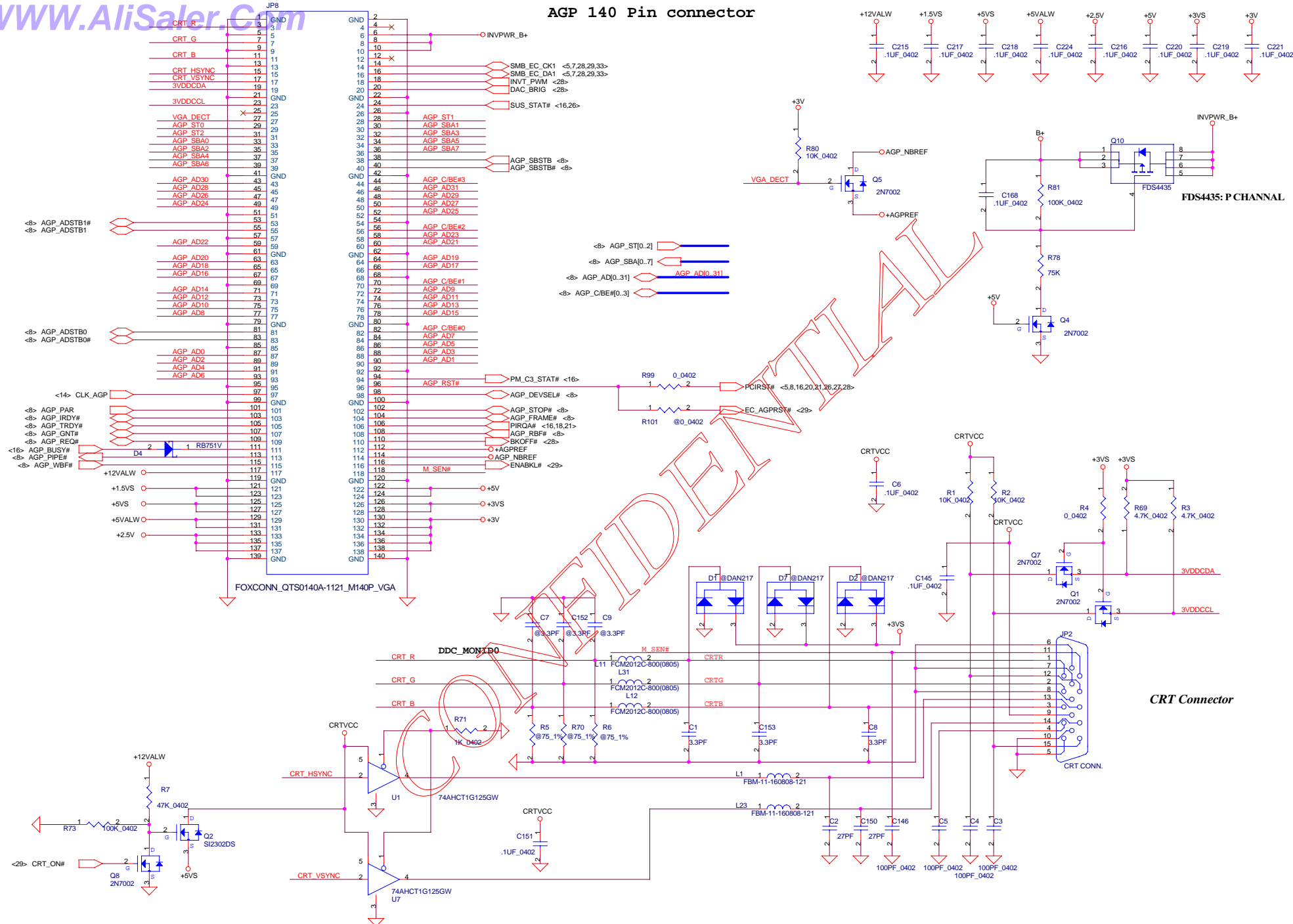
Note:
CPU_CLK[2:0] needs to be running in C3, C4.



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Compal Electronics, Inc.			
Clock Generator			
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AGP 140 Pin connector



Compal Electronics, Inc.

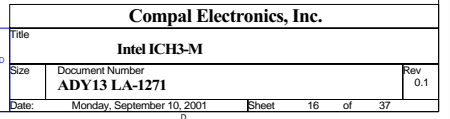
AGPConn. & CRT

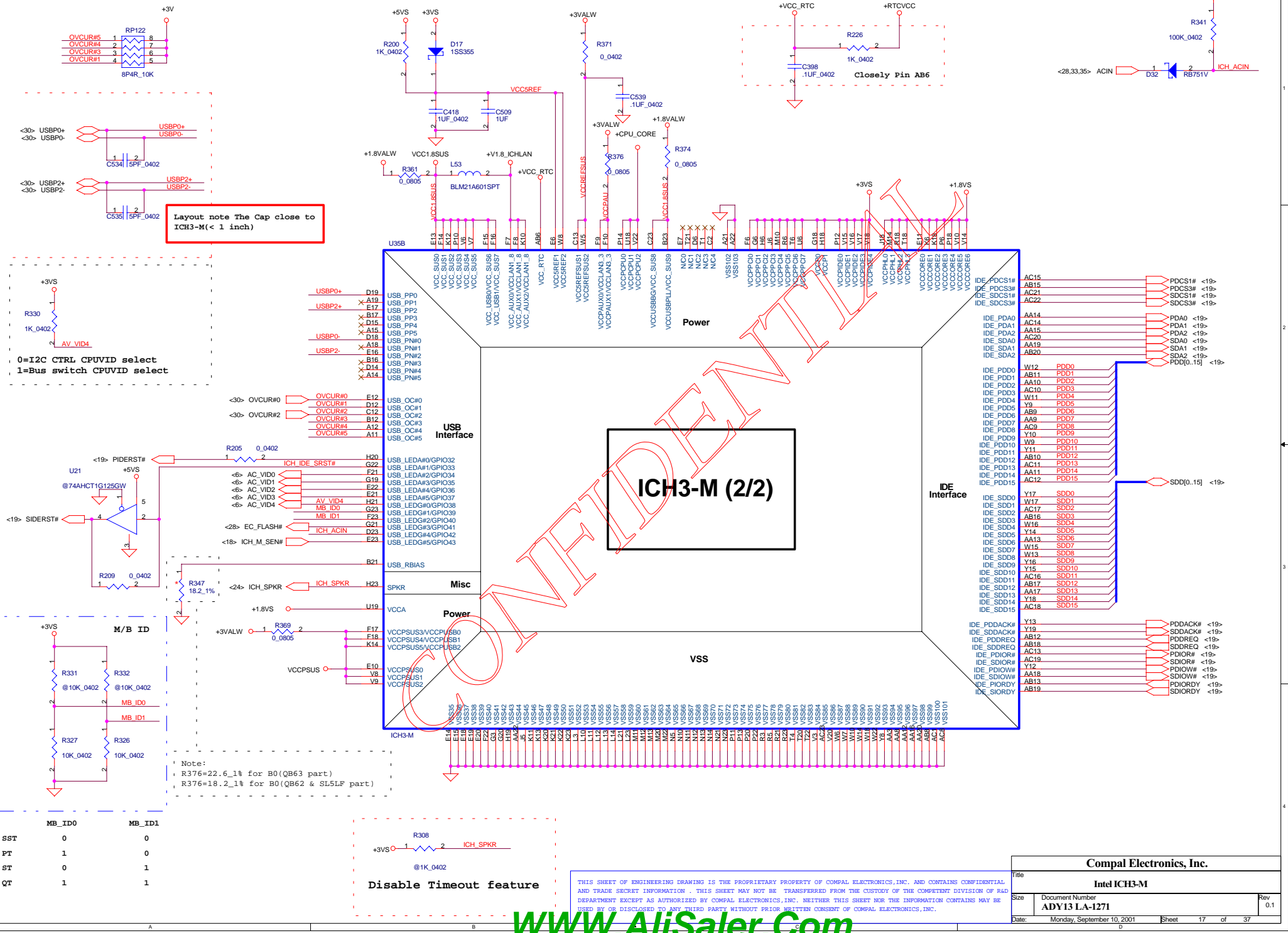
ADY13 LA-1271

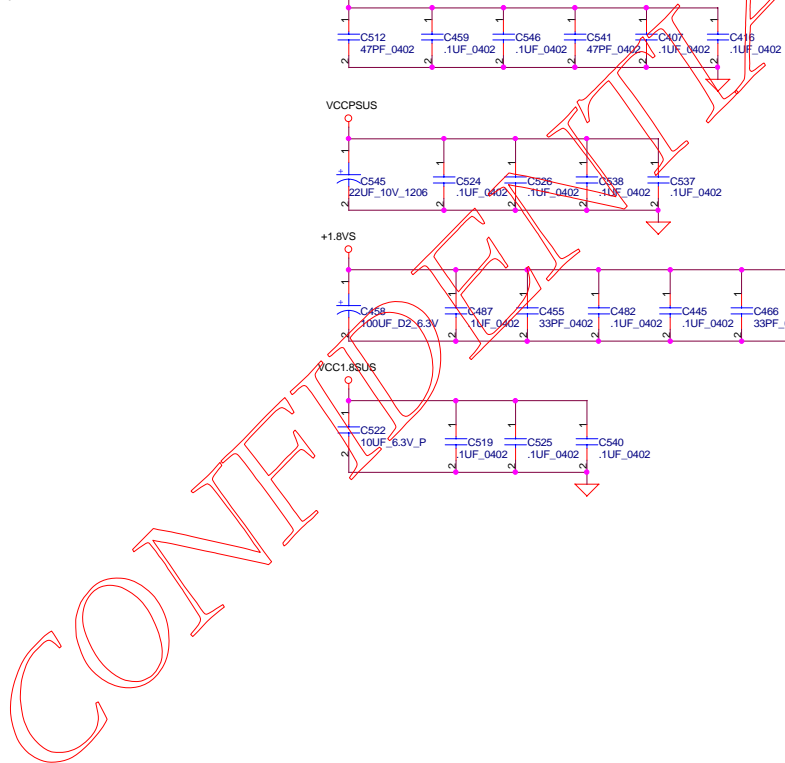
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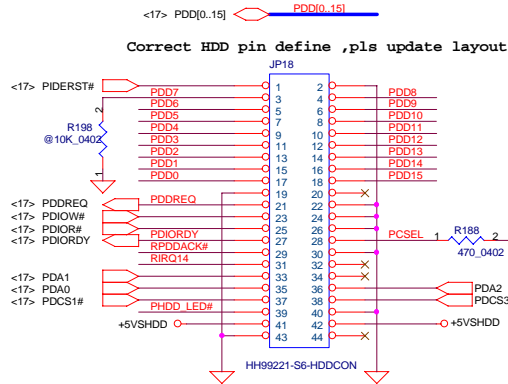




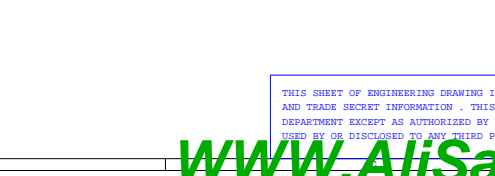
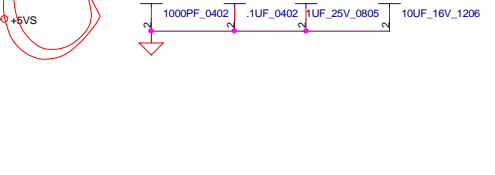
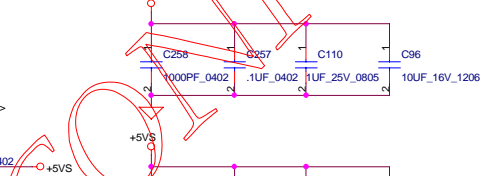
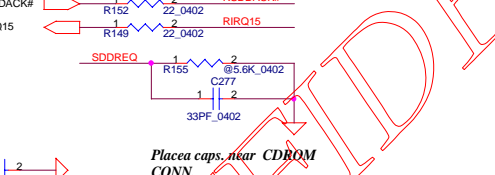
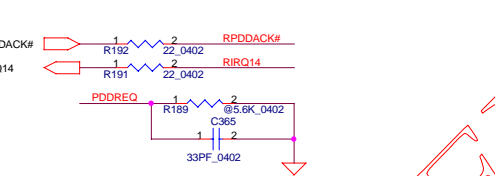
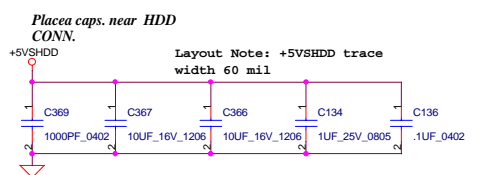
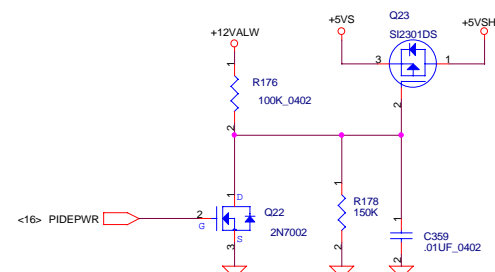
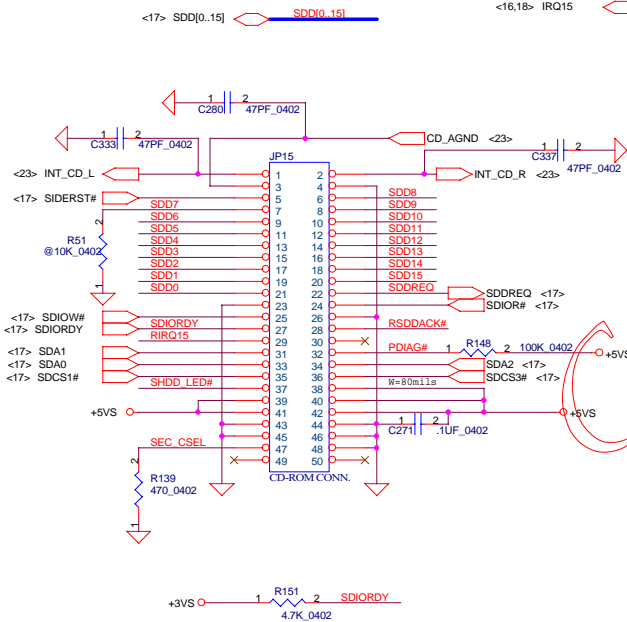


AL R&D ENG	Compal Electronics, Inc.			
	Title ICH3-M Decoupling & Pull-Up			
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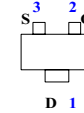
HDD Connector



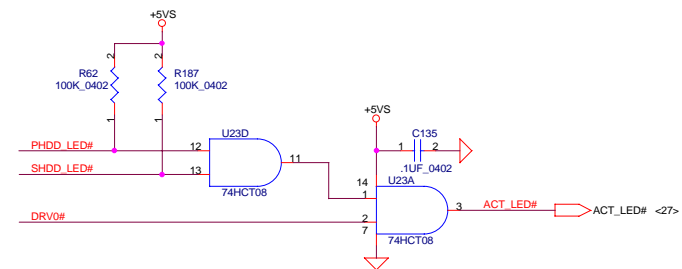
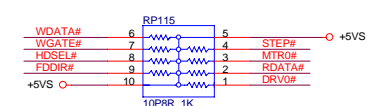
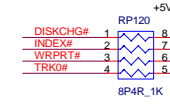
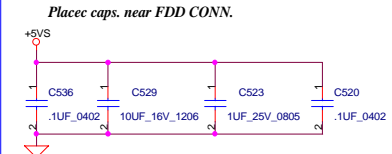
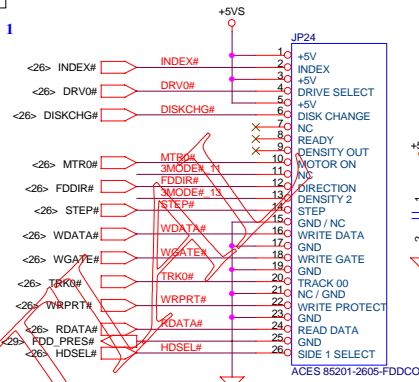
CD-ROM Connector



SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +8V



FDD Connector

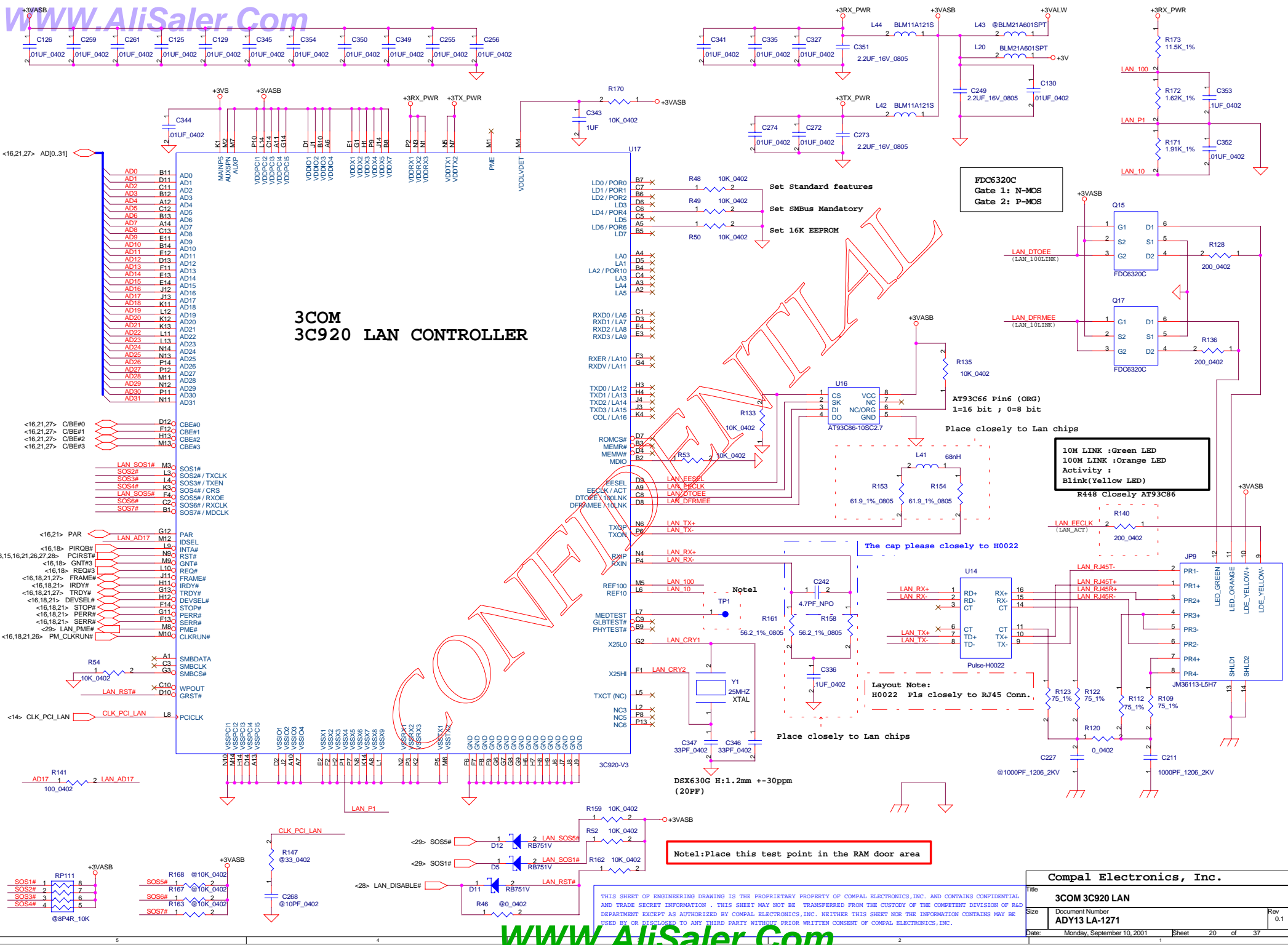


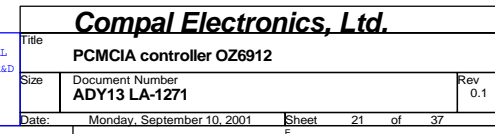
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Compal Electronics, Inc.

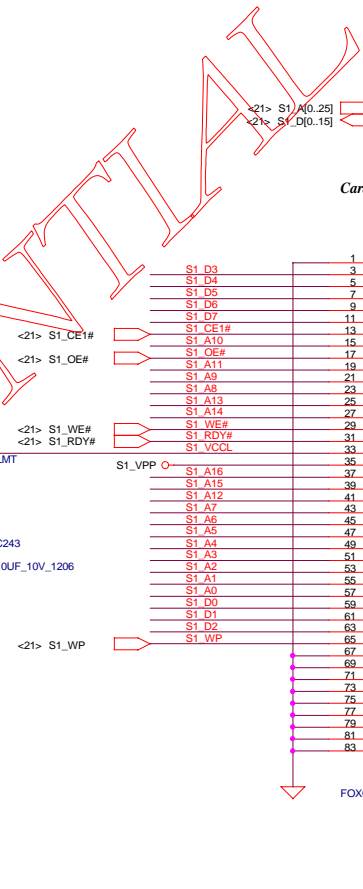
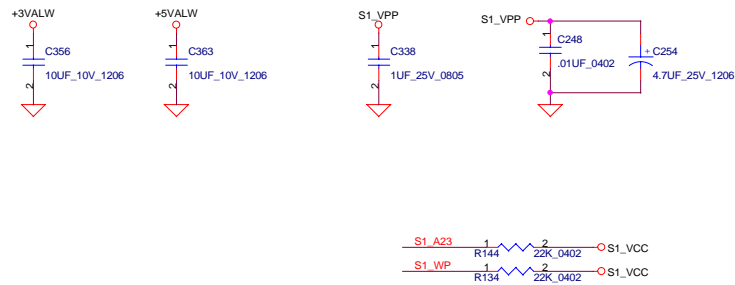
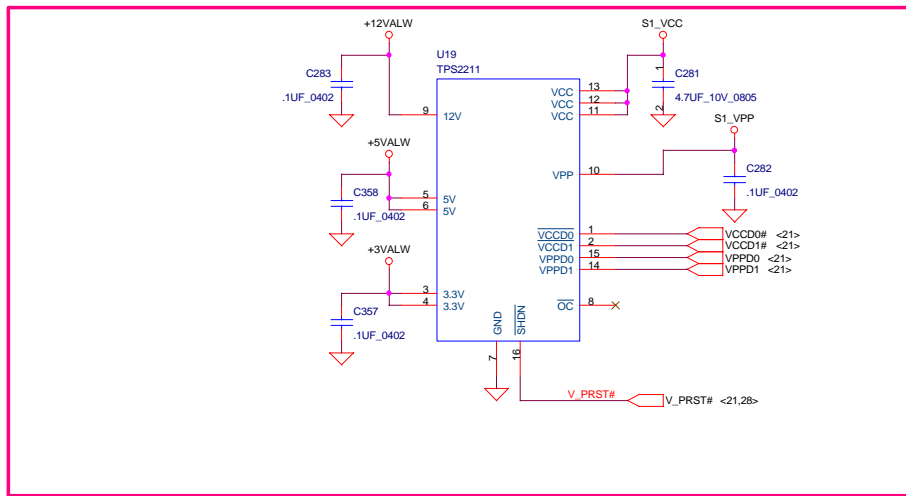
IDE/FDD/CD-ROM Module

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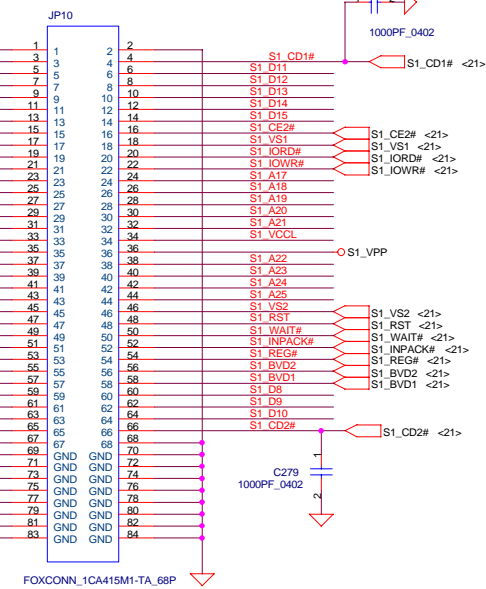




PCMCIA Power Controller

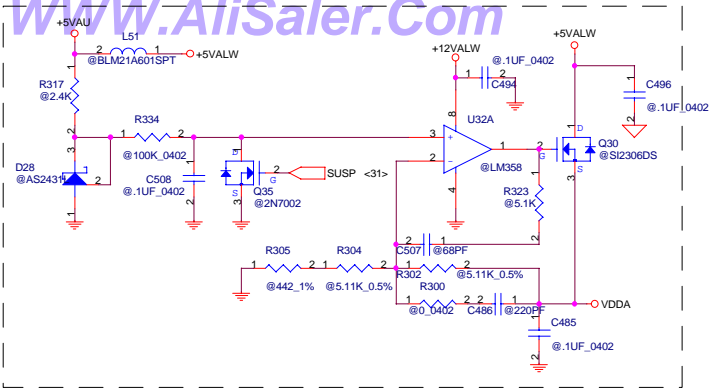


CardBus Socket

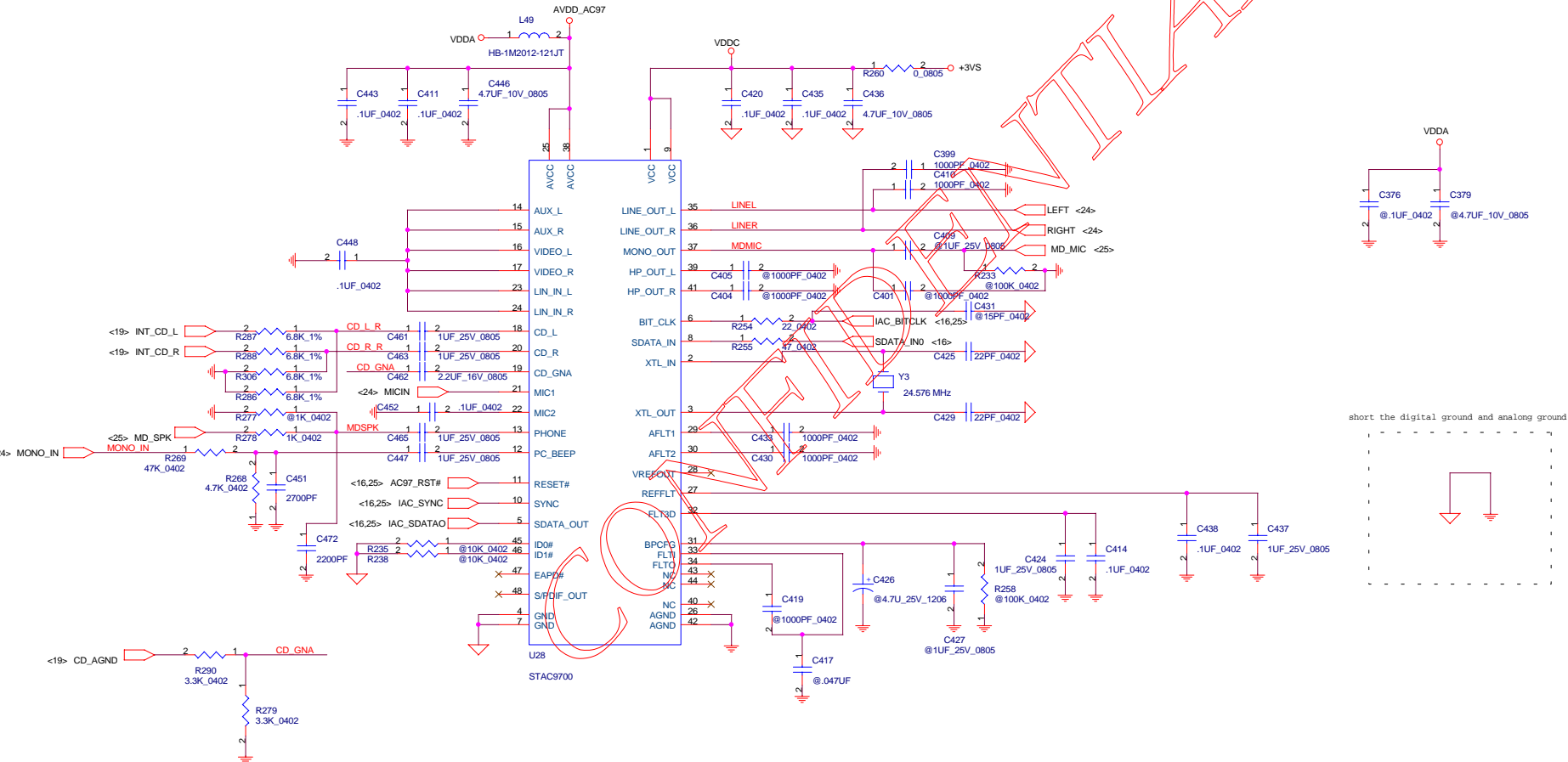
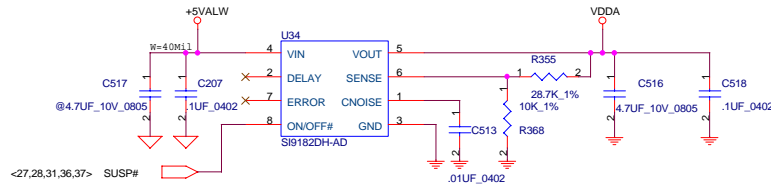


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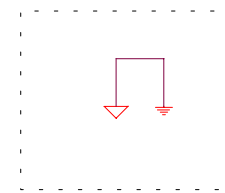
Compal Electronics, Inc.			
CardBus Socket			
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reserve for AC97 coedc using only

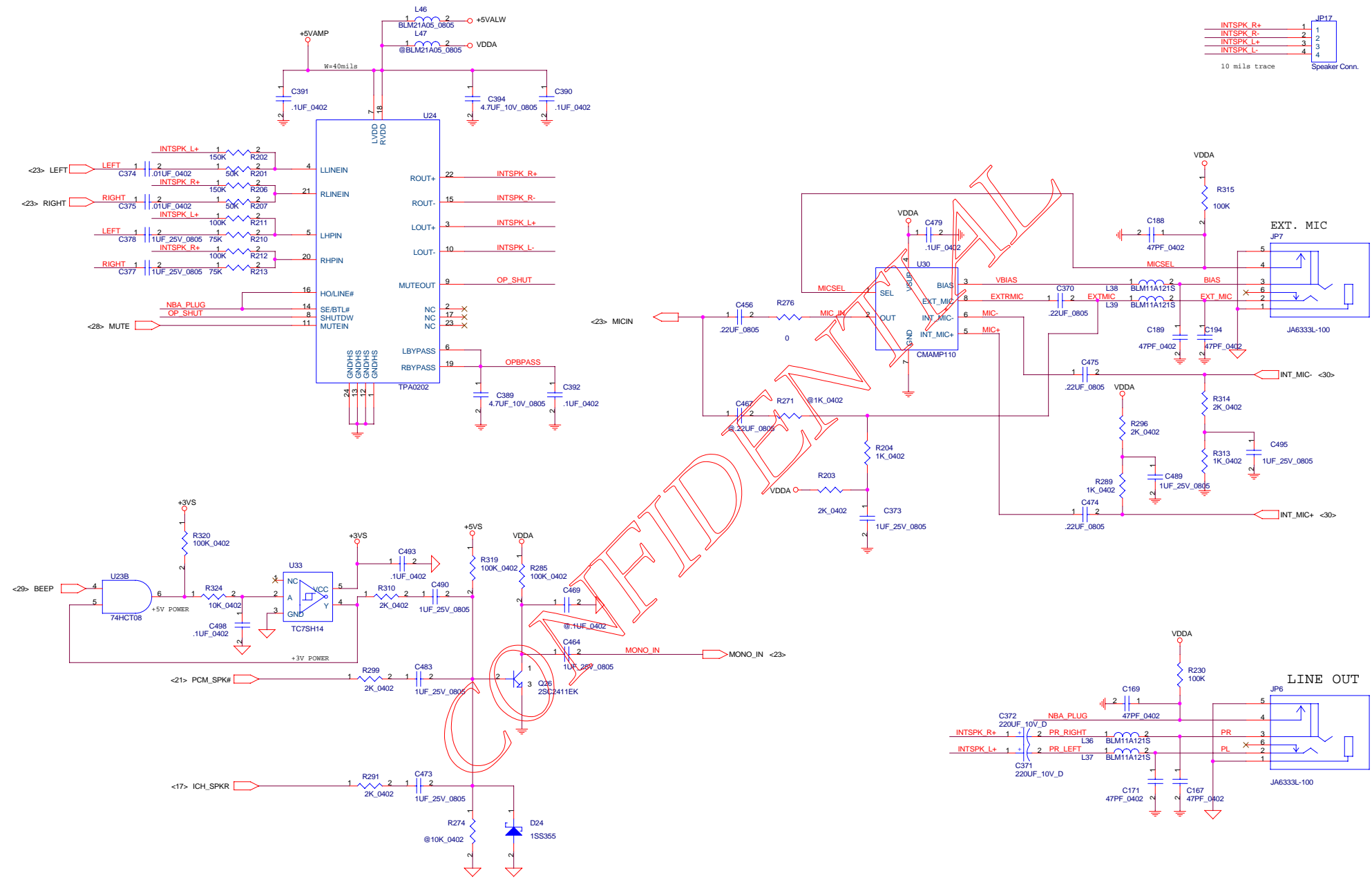


short the digital ground and analog ground



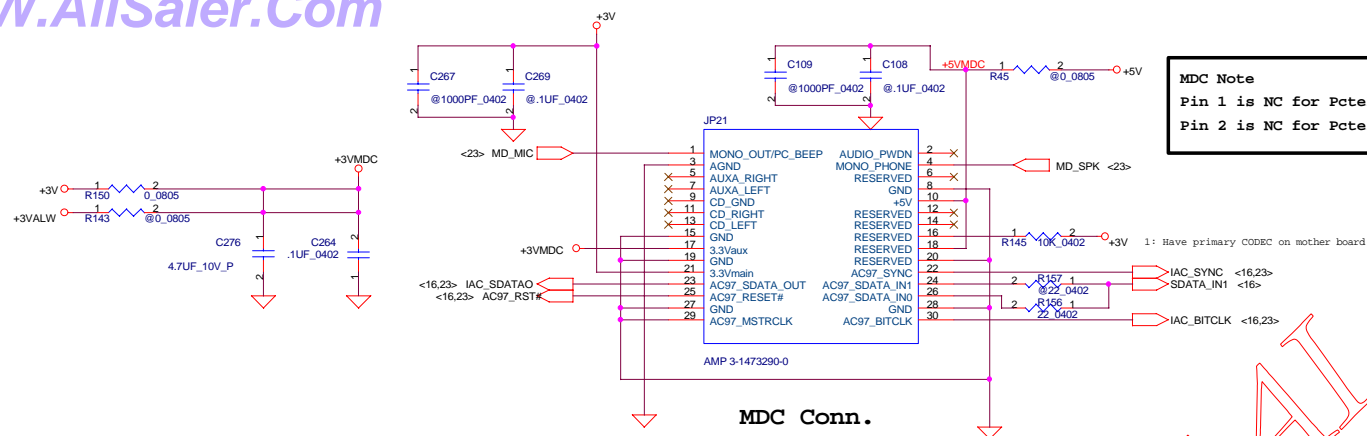
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Compal Electronics, Inc.			
Title			
AC97 CODEC			
Size			
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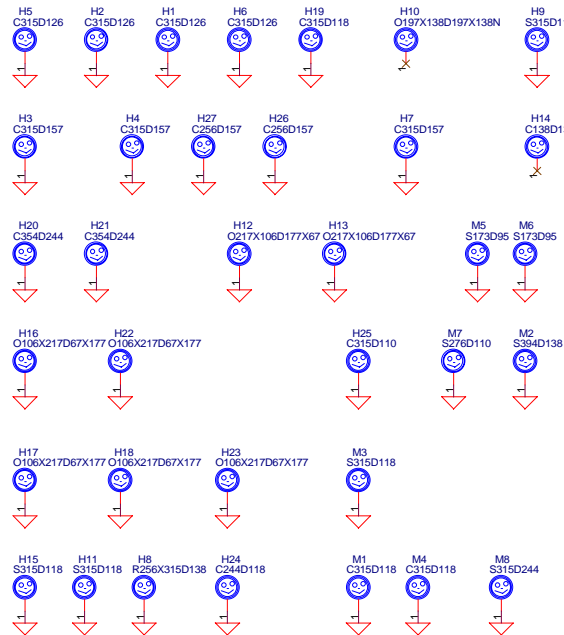
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Compal Electronics, Inc.			
Title			
AMP & Audio Jack			
Size	Document Number	Rev	
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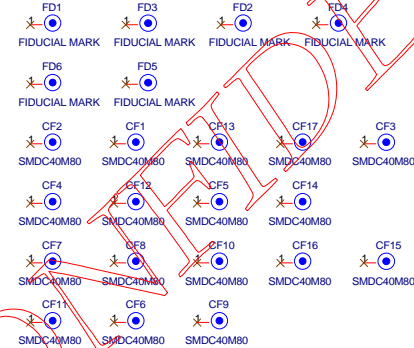


MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

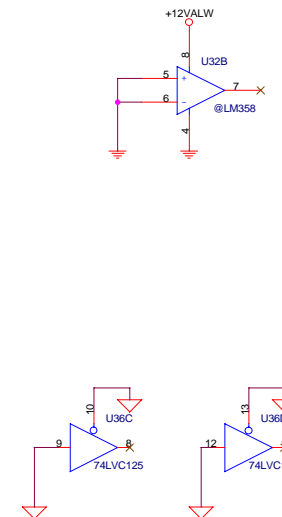
Screw Hole



Fidui al Mark

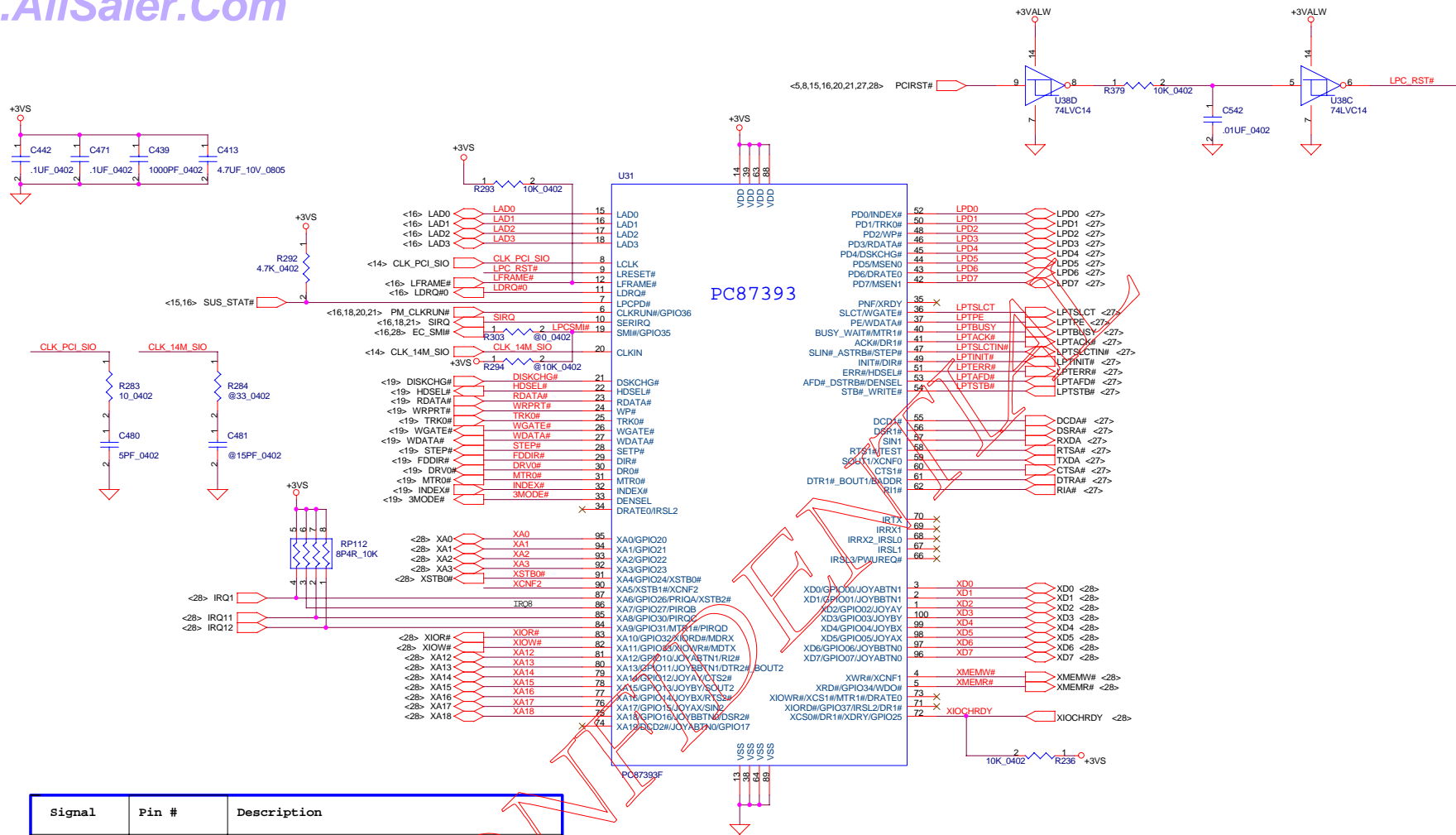


Spare Logic Gate



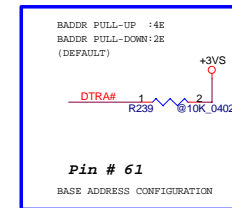
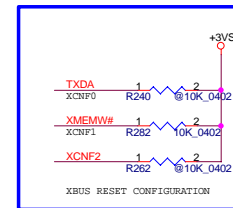
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Compal Electronics, Inc.			
Title			
MDC connector / Skew Hole			
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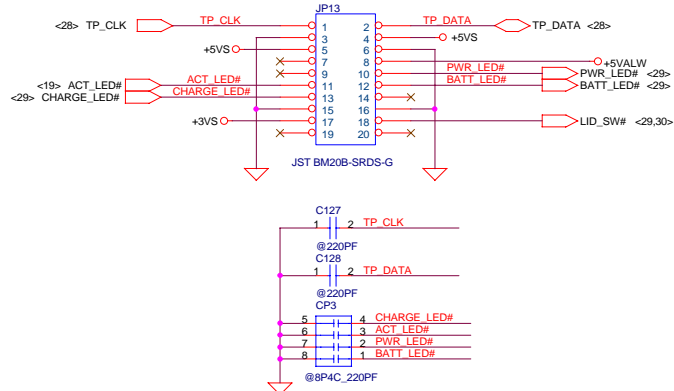
Signal	Pin #	Description
BADDR	61	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F
TEST	58	"0": Normal (Default) "1": Test Mode
XCNF[2:0]	90, 4, 59	2 1 0 Function
		x 0 0 No BIOS
		x 0 1 Normal Mode. XRDY disabled
		(default) 0 1 0 Latch Mode. XA12-19, XRDY enabled
		1 1 0 Latch Mode. GPIO10-17, XRDY enabled
		0 1 1 Latch Mode. XA12-19, XRDY disabled
		1 1 1 Latch Mode. GPIO10-17, XRDY disabled

* 1 ROM SOLUTION

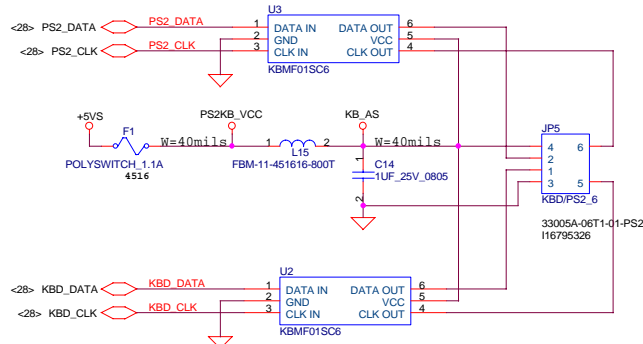


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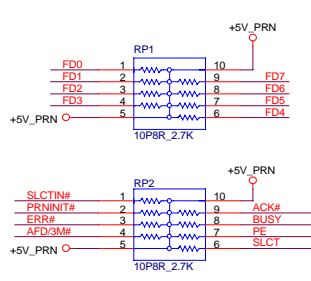
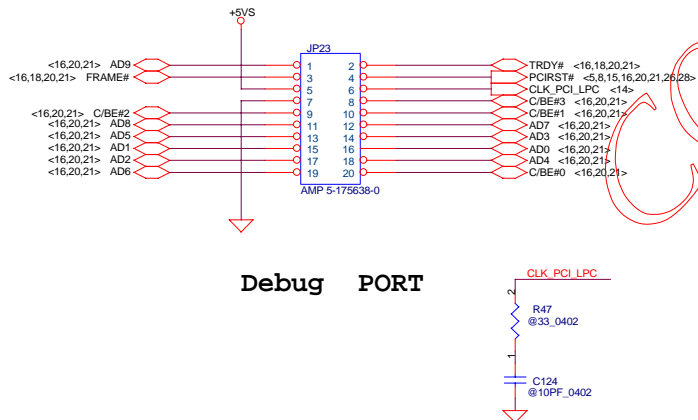
Compal Electronics, Inc.			
Title LPC Super I/O NS PC87393			
Size	Document Number ADY13 LA-1271	Rev 0.1	
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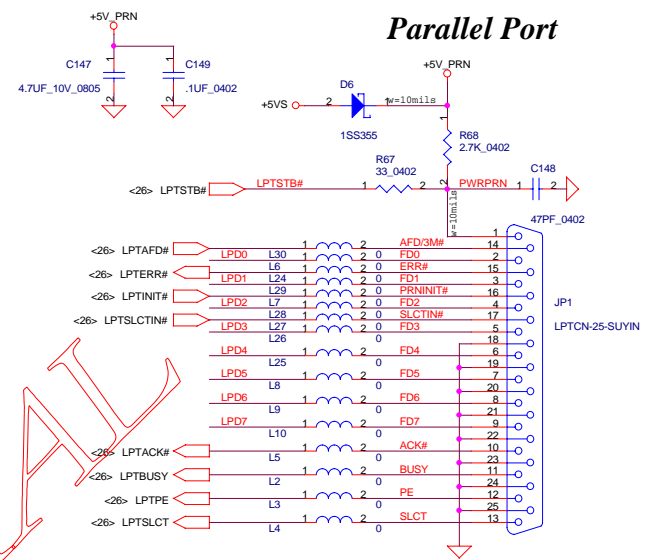
PS2 CONN.



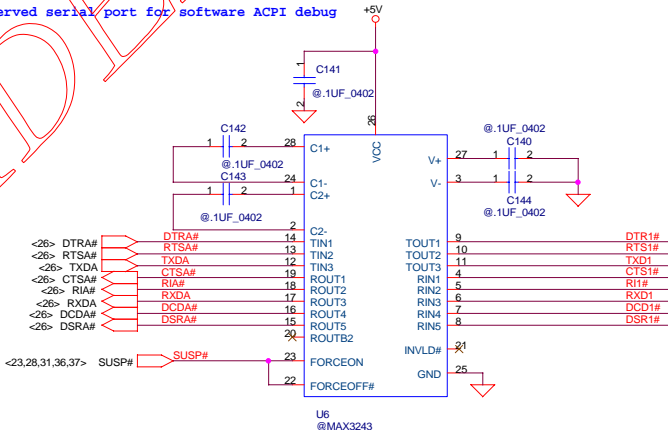
Debug PORT



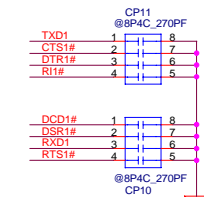
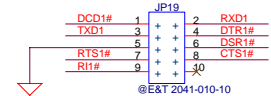
<26> LPD[0..7] LPD0..7



Reserved serial port for software ACPI debug

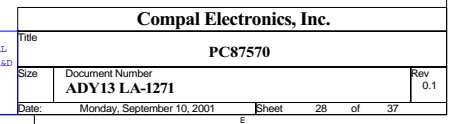


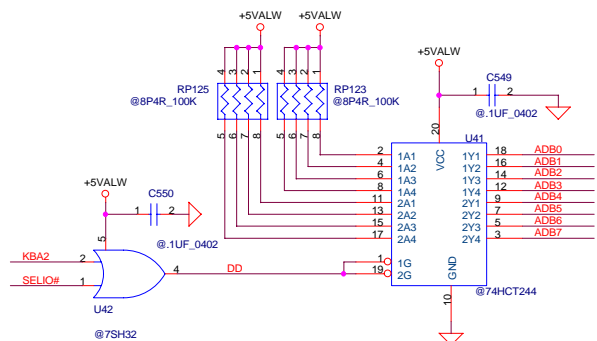
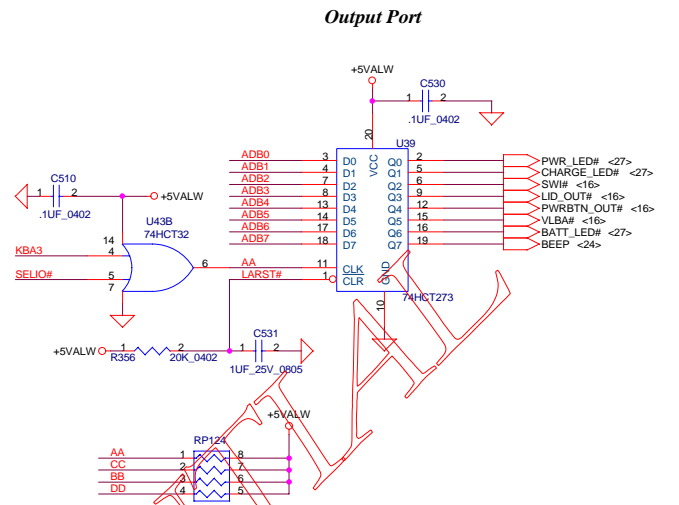
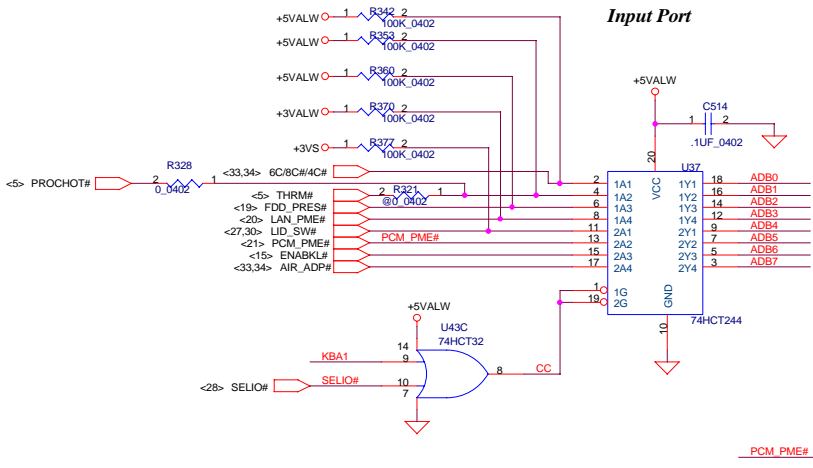
ACPI Debug port



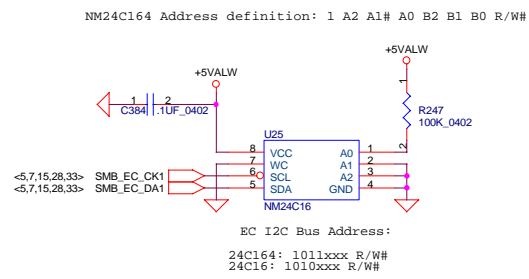
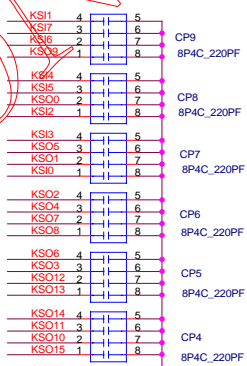
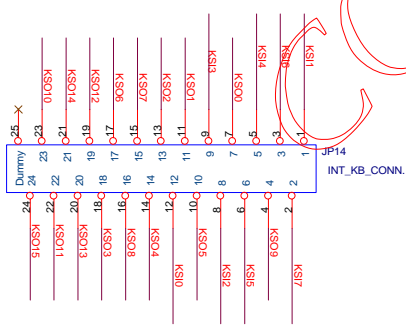
Place close to COM1 connector.

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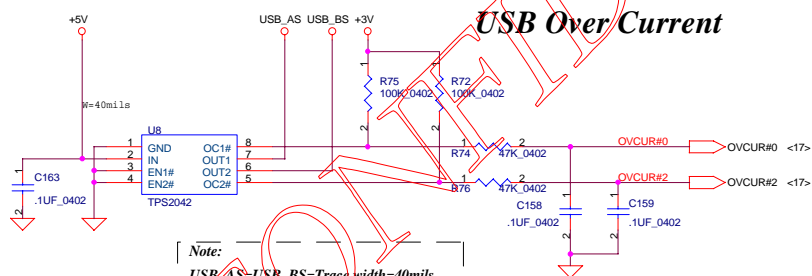
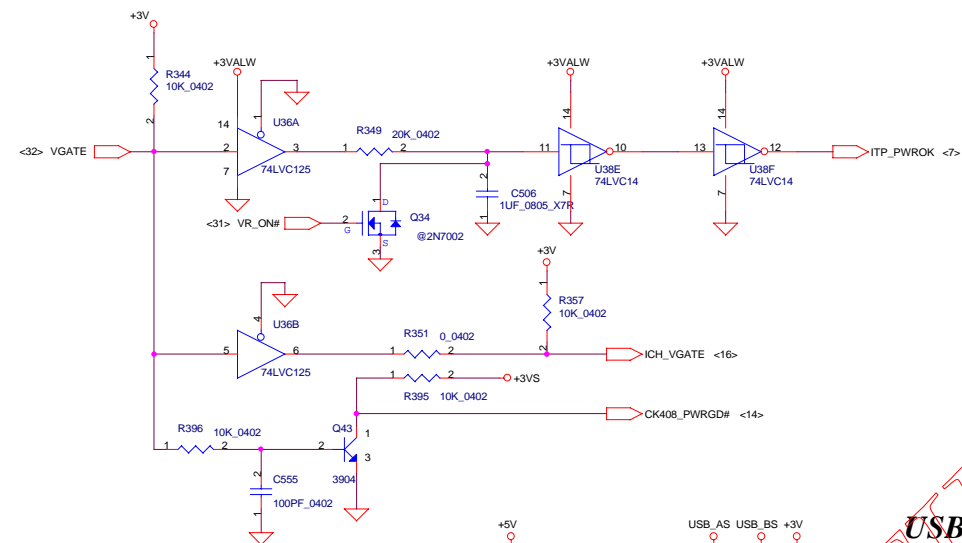
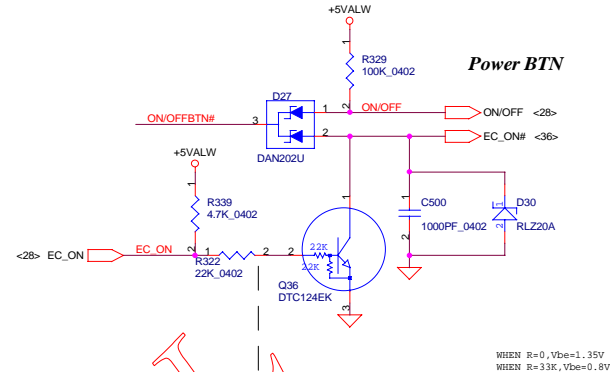
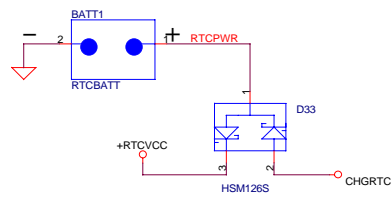
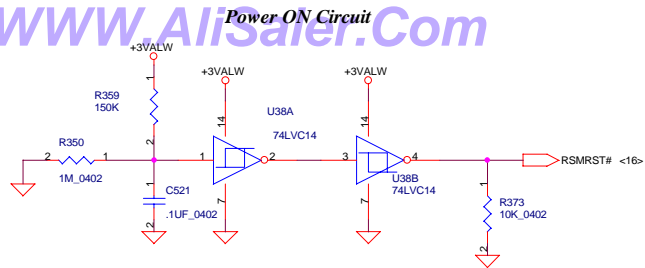


INT_KBD_CONN.

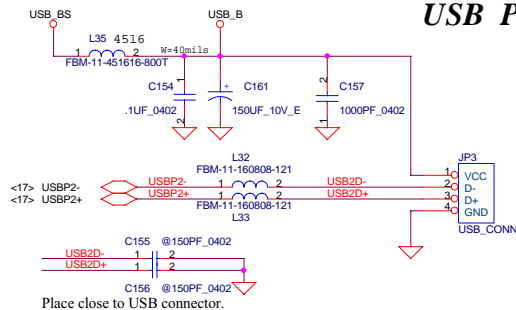
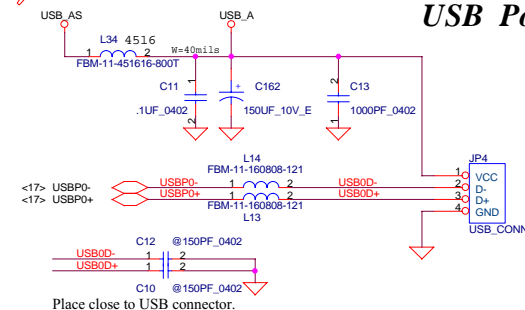
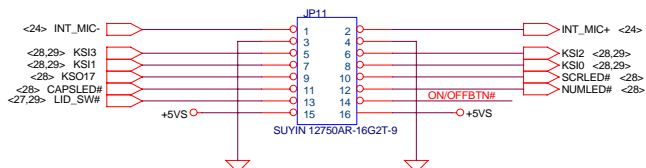


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Compal Electronics, Inc.			
EC Extend I/O KB Conn. & BIOS			
Size	Document Number	Rev	
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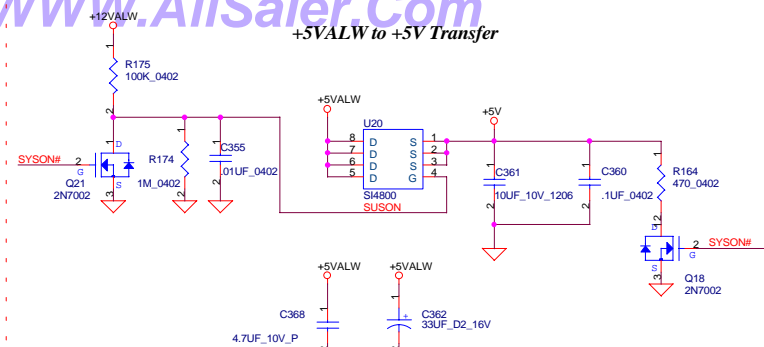
Note:
USB_AS=USB_BS=Trace width=40mils



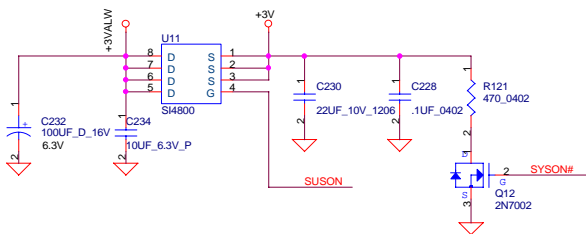
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Title			
Power OK/Reset/RTC battery/USB Conn.& Lid Switch			
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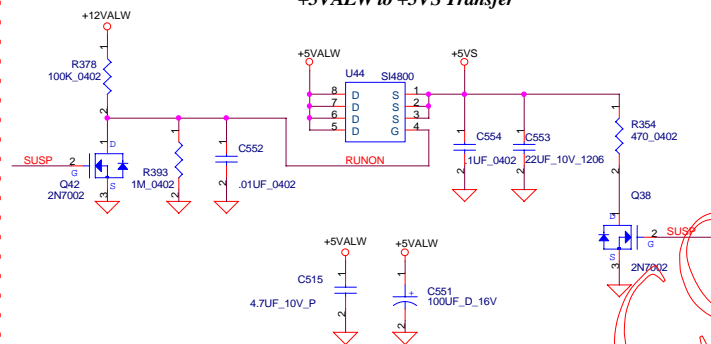
+5VALW to +5V Transfer



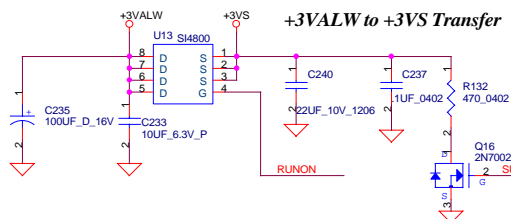
+3VALW to +3V Transfer



+5VALW to +5VS Transfer

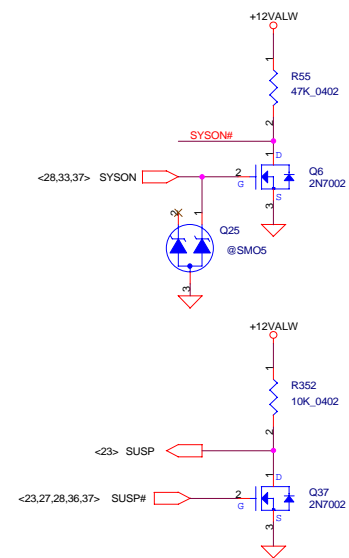
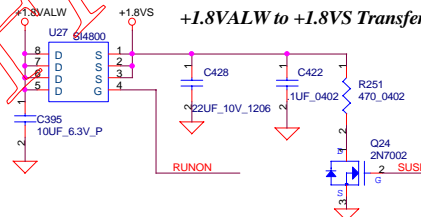


+3VALW to +3VS Transfer



1.8VALW/+1.5VS Power direct provide

+1.8VALW to +1.8VS Transfer



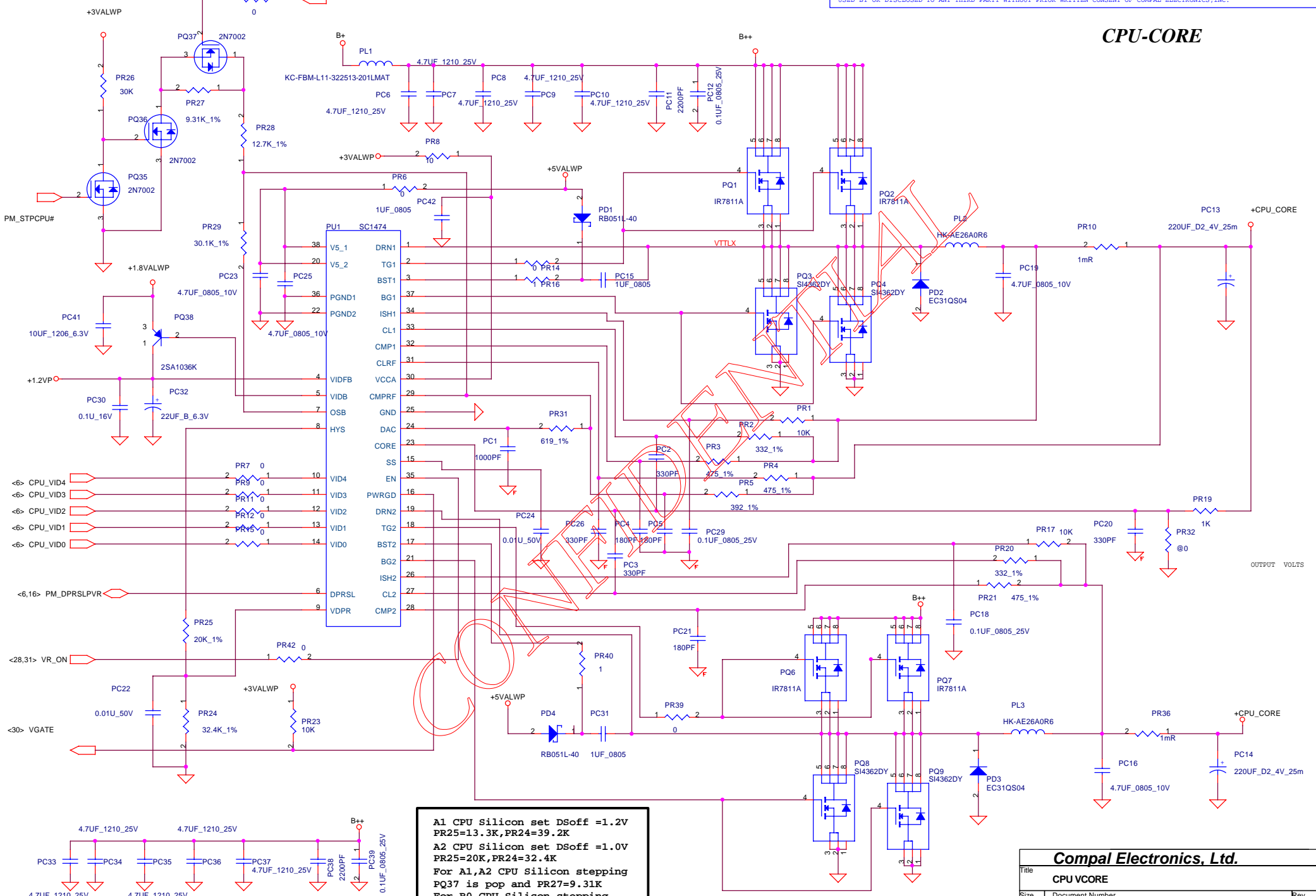
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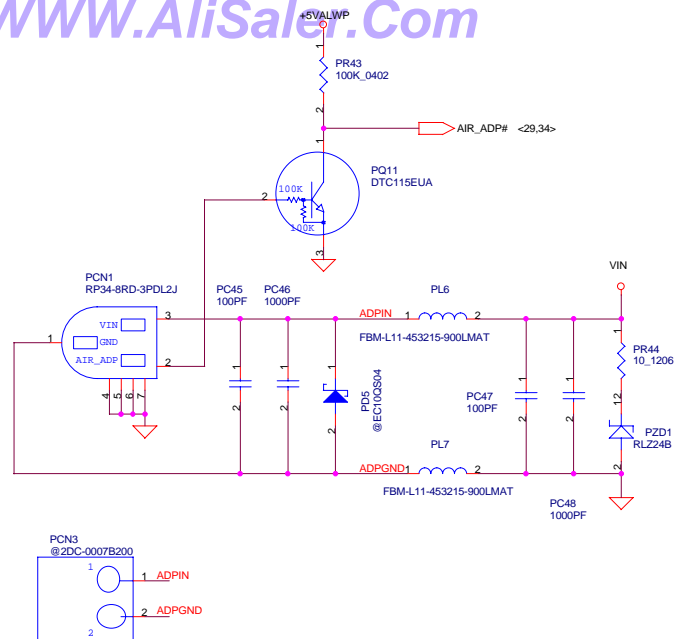
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DC/DC Circuit

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Compal Electronics, Ltd.			
Title			
CPU VCORE			
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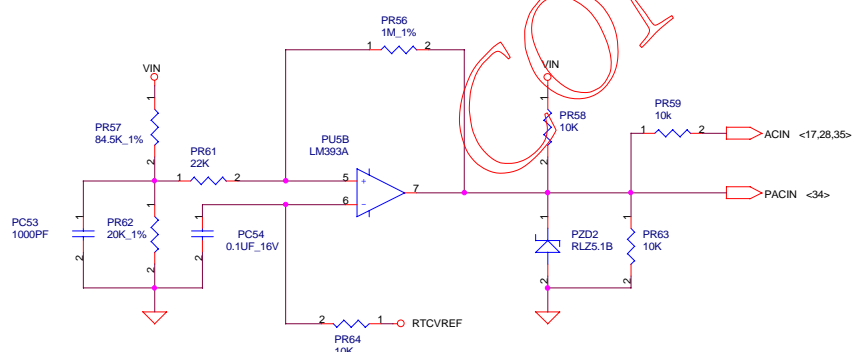


PCN2 battery connector pin assignment

SMART Battery:

- 1.BAT+
- 2.LI/MH#
- 3.B/I
- 4.TS
- 5.SMB_EC_DA1
- 6.SMB_EC_CK1
- 7.GND

Vin Detector
17.93V/17.2V



Precharge detector
15.9V/13.2V FOR
ADAPTOR

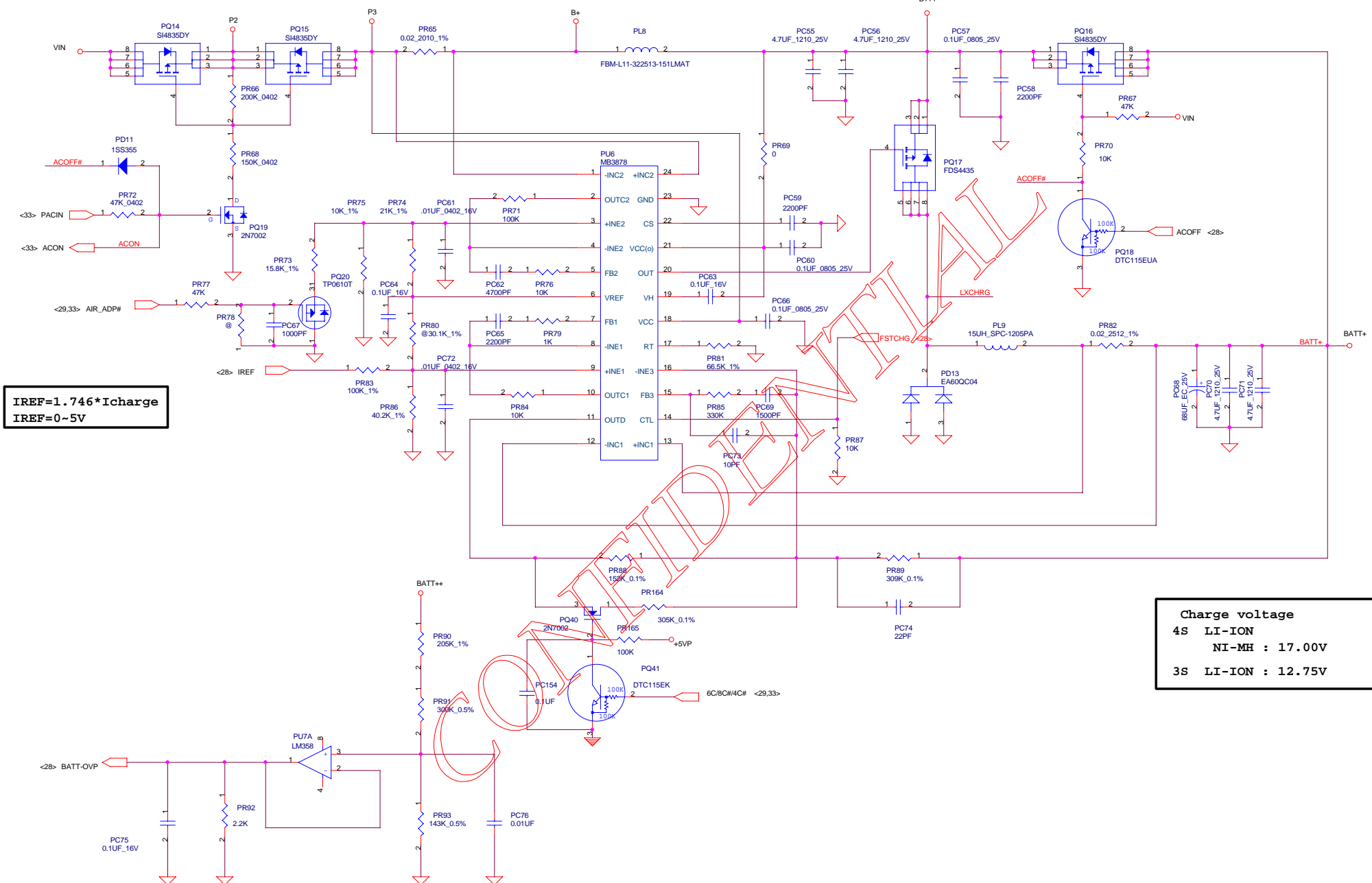
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Compal Electronics, Inc.		
Title	Detector	
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Iadp=0~3.22A
Iair=0~2.26A

<-----Actually about 3A

Charger



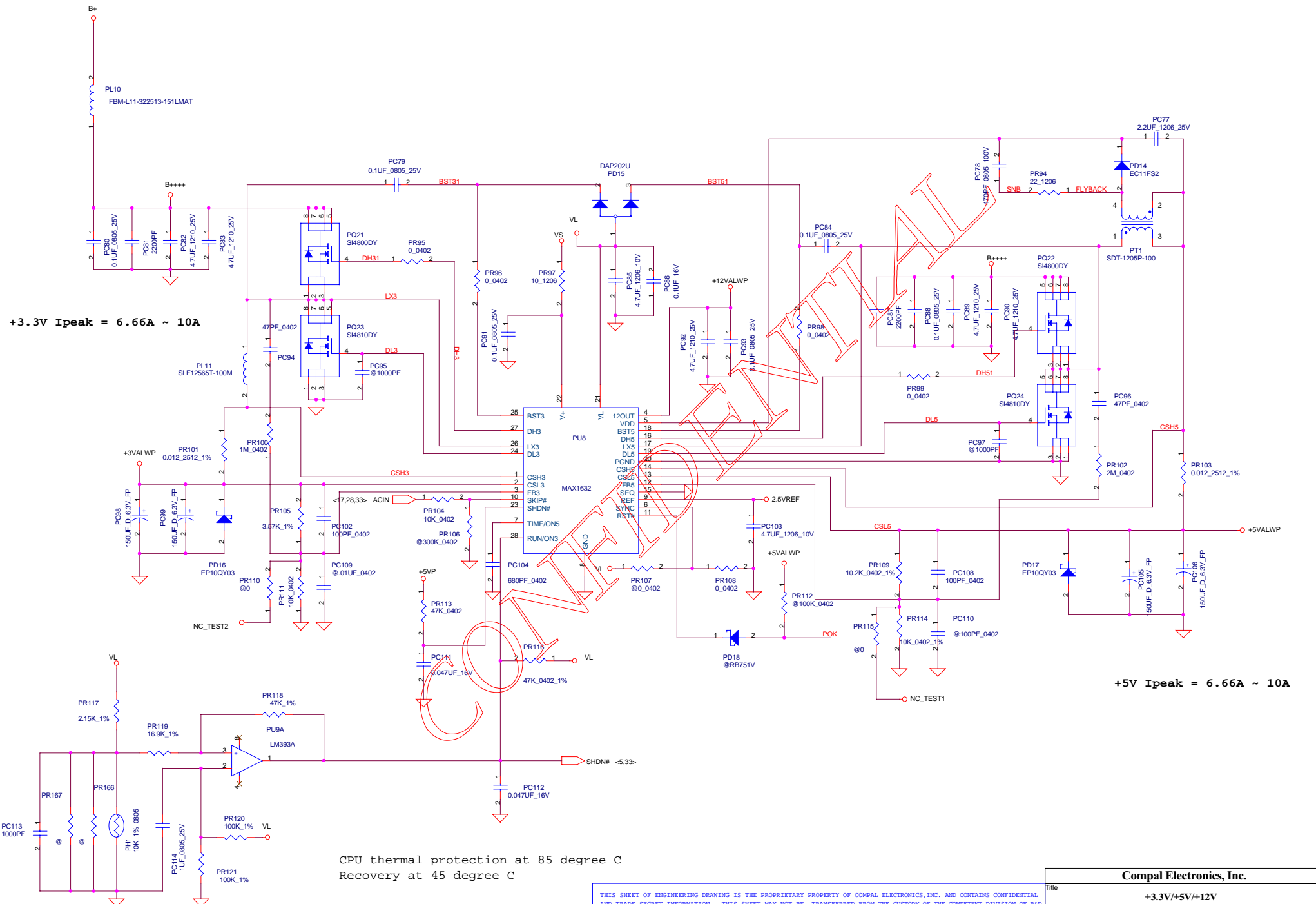
IREF=1.746*Icharge
IREF=0~5V

Charge voltage
4S LI-ION
NI-MH : 17.00V
3S LI-ION : 12.75V

OVP voltage :
LI-4S : 18.3V----BATT-OVP=4.04V
LI-3S : 13.5V----BATT-OVP=3.82V
BATT-OVP=0.2206*BATT++

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Compal Electronics, Inc.		
Charger		
Size	Document Number	Rev
	ADY13 LA-1271	0.1
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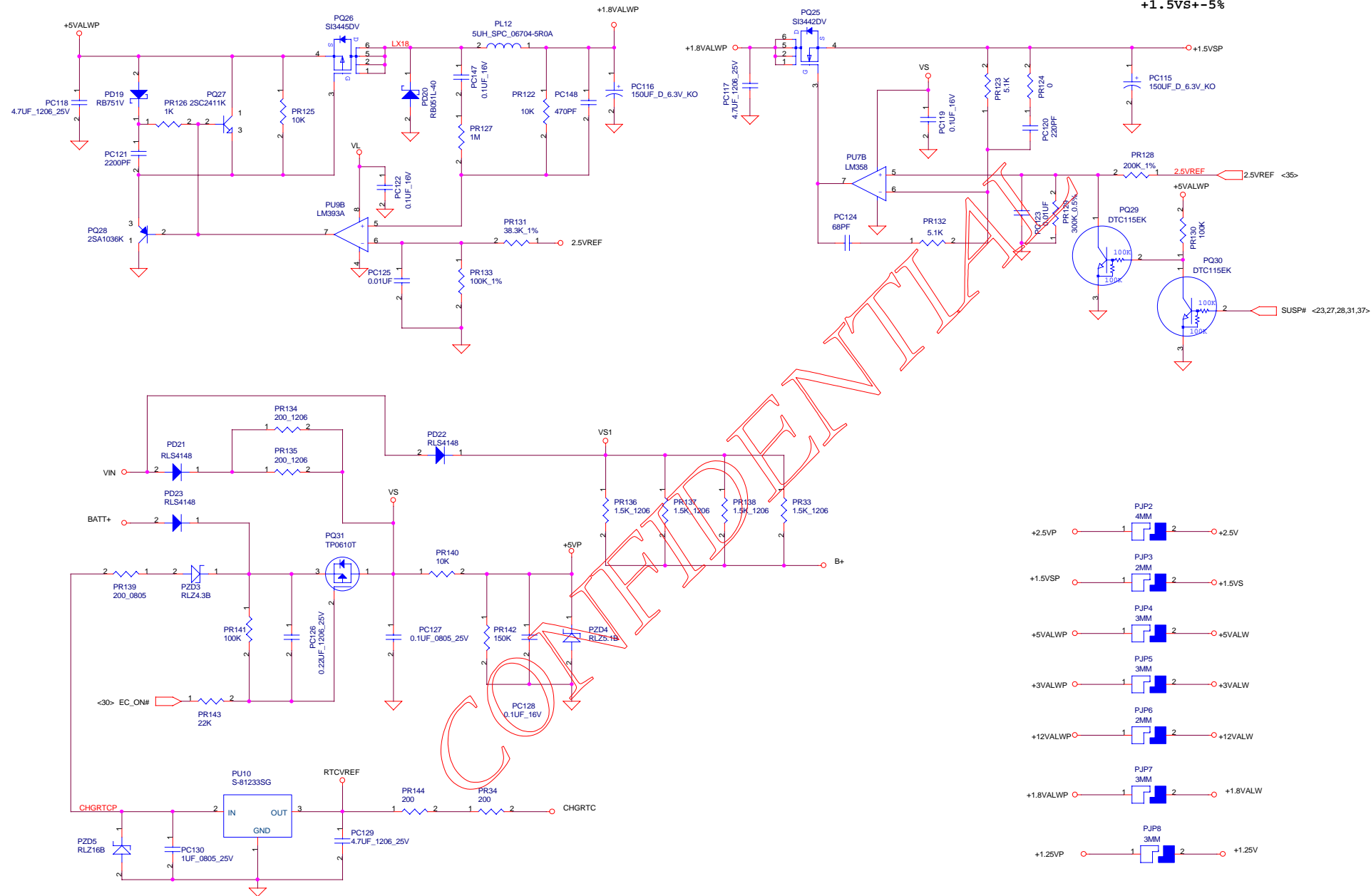


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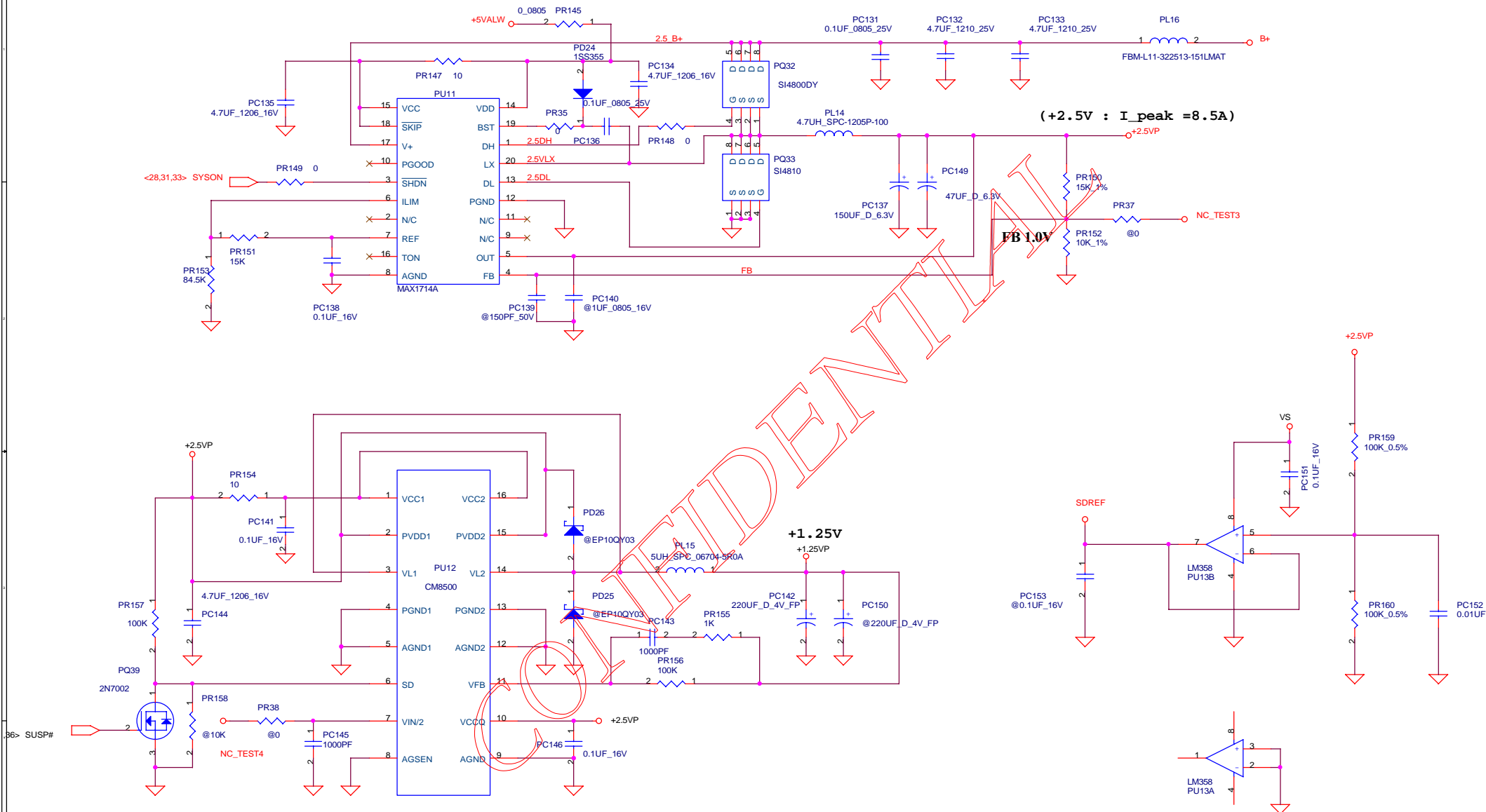
Compal Electronics, Inc.		
Title	+3.3V/+5V/+12V	
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+1.8V+-5%

+1.5VS+-5%



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